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【1】Functional Explanation

1-1 Abstract

GP2AP002S00F makes successive binary decisions whether reflective object exists, which GP2AP002S00F irradiates IR light to and receives its reflection from, according to its internal algorithm. GP2AP002S00F controls a built-in IR LED, irradiating time-varying pulse train which consists of elementary pulse having approximately 8 us duration. The number of pulses is at most three in one detection cycle (fundamental detection period is approximately 8ms). Also, GP2AP002S00F detects reflection of these optical pulses synchronously and asynchronously to LED emission in order to make such decisions.

The basic algorithm used in GP2AP002S00F to detect existence or absence of object is as follows.
<When proximity state (sensing result) changes from “no detection” to “detection”>
3-consective synchronous “true” detection of reflected optical pulses : detection of object existence
the other cases : no detection of object existence
<When proximity state (sensing result) changes from “detection” to “no detection”>
3-consective synchronous “false” detection of reflected optical pulses : detection of object absence
the other cases : no detection of object absence

GP2AP002S00F has internal registers to setup its functions in order to properly detect natural movement of the human body. Following parameters are available to setup through I^2C bus interface.

1-1-1 Output method control
Sensing result of the proximity is always output to the register PROX (ADDRESS 00H)’s VO bit.
On the other hand, the output method of Vout terminal can be switched over between two kinds of operation, Normal output mode and Interrupt output mode. See 1-4 and【2】for more detail.

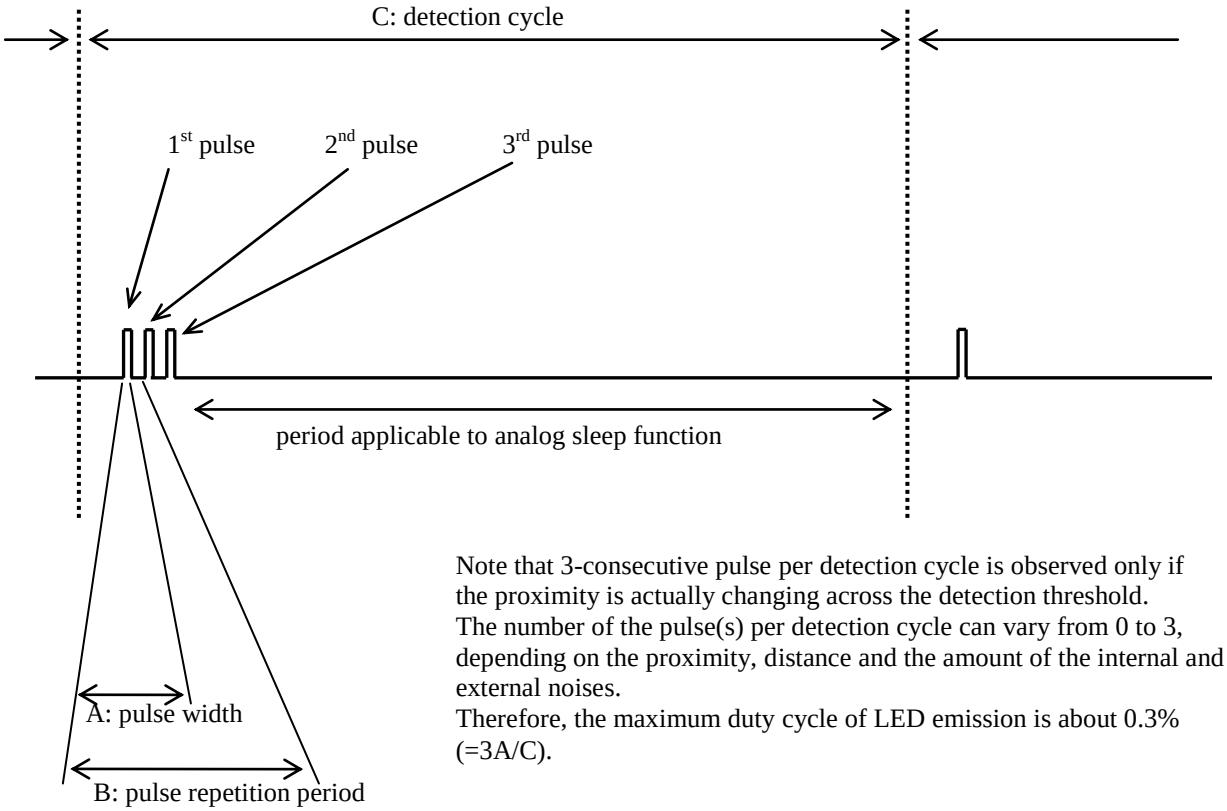
1-1-2 Software shutdown function
GP2AP002S00F has shutdown function by which all analog circuits go into shutdown mode and cease to draw supply current. Current consumption of GP2AP002S00F in shutdown mode, Icc-s, is less than 1uA when I^2C bus interface is not used.

1-1-3 Detection distance and Detection distance hysteresis
The sensitivity of GP2AP002S00F can be optimized by HYS register setting, resulting in intended range of detection distance and its hysteresis characteristics. Note that the detection distance depends both on the sensitivity and the peak power of LED emission. The latter is determined by current limiting resistor, RLED. See【2】and【3】for more detail.

1-1-4 Detection cycle (response time)
Fundamental detection period of GP2AP002S00F is approximately 8 ms. The detection cycle can be extended up to approximately 1 second by CYCLE register setting. The longer the detection cycle, the lower the LED average current consumption, but the longer the response time, too. Please make sure validity of the detection cycle setting in accordance with your own system. See 1-8 and 1-9 for more detail.

1-1-5 Analog sleep function
Under continuous operation, analog sleep function helps reduce average current consumption through Vcc terminal (except for the one through VLED terminal). This function differs from 1-1-2 software shutdown function, de-activating internal analog circuit intermittently and partly. See 1-7 and 1-9 for more detail.

The figure below shows the relationship between LED emission timing and detection cycle.
A pulse width. Typically ~ 8us.
B pulse repetition period. Typically ~ 0.1ms.
C detection cycle. Typically ~ 8ms. (initial setting)



Note that 3-consecutive pulse per detection cycle is observed only if the proximity is actually changing across the detection threshold.
The number of the pulse(s) per detection cycle can vary from 0 to 3, depending on the proximity, distance and the amount of the internal and external noises.
Therefore, the maximum duty cycle of LED emission is about 0.3% (=3A/C).

1-2 I^2C bus interface

GP2AP002S00F operates as a slave device on the I^2C bus interface, having a 7-bit-slave address. Through the SDA and SCL terminals, GP2AP002S00F's registers can be set up, and also GP2AP002S00F's sensing result can be read out. However, the read format specified for GP2AP002S00F differs from the normal read format (immediately after the first byte) or the combined format shown in the I^2C-bus specification. It is recommended that proper operation procedures be implemented according to each host system's requirements by consulting with 1-2-2 and【2】.

The dedicated terminals for the I^2C bus interface are listed below.

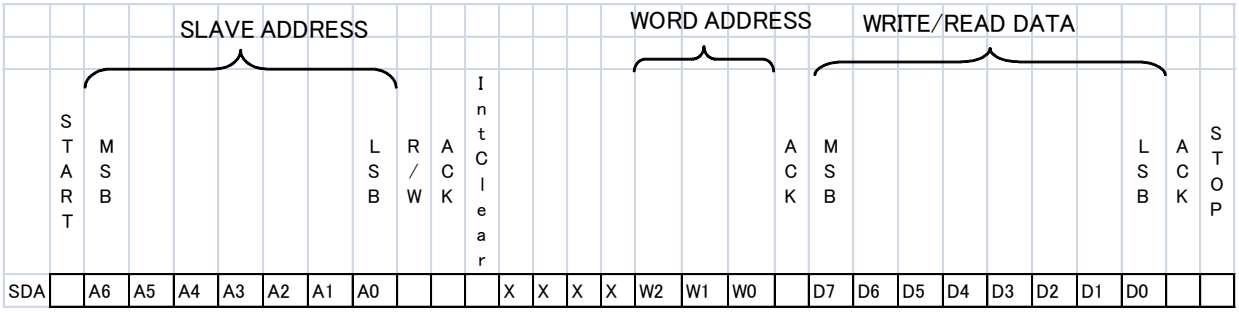
Pin name	Description
SCL	I^2C Clock
SDA	I^2C Data bus

Fundamental data formats for GP2AP002S00F are as follows.

SLAVE ADDRESS :

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	0	0	X

R/W : Read : X=1, Write : X=0
WORD ADDRESS : In writing GP2AP002S00F's register, the corresponding word address can be selected by a combination of three bits, W0 to W2. In reading GP2AP002S00F's register, the word address need not be designated. See also "Internal Register Map".
WRITE/READ DATA : Data to be written into / read from the corresponding register.
IntClear : A flag to clear an interruput signal. It is only effective when Vout terminal operates in "interrupt" mode.
IntClear is available in the both formats shown below. See 1-4 and【2】for more detail .



1-2-1 Write Format

SDA data format to be used in writing a GP2AP002S00F's register is as follows.

bit width	1	7	1	1	1	4	3	1	8	1	1
	S	Slave Address	0	A	IntClear	XXXX	Word Address	A	Write Data	A	P

A: Ack, S: Start, P: Stop, X: Don't care

IntClear: 1: Clear Interrupt, 0: Don't Clear Interrupt

□: Master ■: Slave

The word address 00H is for read-only.

1-2-2 Read Format (*)

SDA data format to be used in reading a GP2AP002S00F's register is as follows.

bit width	1	7	1	1	1	7	1	7	1	1	1
	S	Slave Address	1	A	IntClear	XXXXXXX	A	1111111'b	VO	A/NA	P

A: Ack, NA: Nack, S: Start, P: Stop, X: Don't care

IntClear: 1: Clear Interrupt, 0: Don't Clear Interrupt

VO: Proximity sensing result

□: Master ■: Slave

There is only one word address 00H, PROX register, to be read out, so the word address need not be designated as long as R/W is set to 1 (read). The VO bit expresses the latest proximity sensing result. It is forbidden to try overwritng the VO bit. The other data bits in 00H register are not to be used.

(*) GP2AP002S00F's read format is in a particular configuration that, in the 2nd byte, IntCleat bit is written from master to slave just before reading VO bit in the 3rd byte. For some host systems, it may be difficult to implement such a read format Even if this is the case, it is possible to let GP2AP002S00F operate properly by implementing the operation procedure described in 2-3-2

1-3 Internal Register Map

When Vcc power supply is turned on, GP2AP002S00F starts up with internal power-on reset function, whichinitializes all the register bit to 0. Also, after Vcc power supply is turned on, and stabilized at over 90% of its final level, it is desirable for the host system of GP2AP002S00F to afford some time margin of about 1ms before issuing read/write commands for these registers.

ADDRESS		SYMBOL	DATA								Initial Value	R/W
			D7	D6	D5	D4	D3	D2	D1	D0		
0	00H	PROX								VO	H'00	R
1	01H	GAIN					LED[0]				H'00	W
2	02H	HYS	HYSD	HYSC[1]	HYSC[0]		HYSF[3]	HYSF[2]	HYSF[1]	HYSF[0]	H'00	W
3	03H	CYCLE			CYCL[2]	CYCL[1]	CYCL[0]	OSC[2]			H'00	W
4	04H	OPMOD				ASD			VCON	SSD	H'00	W
6	06H	CON				OCON[1]	OCON[0]				H'00	W

Not available. All the bits (other than in address 00H) should be set to "0".

VO : Proximity sensing result (0: no detection, 1: detection). It is forbidden to try overwriting the VO bit.
LED[0] : Select switch for LED driver's On-resistance (0: 2x higher, 1: normal setting). Use LED[0]=1.
HYSD, HYSC,HYSF: A set of these bits adjusts the receiver sensitivity, determining characteristics of the detection distance and its hysteresis. For more details on the recommendations for GP2AP002S00F's operation modes and the corresponding register settings, see 1-6 and【2】.
Note that any register setting other than the above recommendations may lead to unspecified / unexpected operation of GP2AP002S00F.
OSC[2] : Select switch for internal clock frequency hopping (0: effective, 1: Not effective). Use OSC[2]=1setting.
CYCL[2:0] : Determine the detection cycle. Starting from 1x (initial setting) of fundamental detection period (typically 8ms), up to 128x extention is possible. See 1-7 for more detail.
SSD : Software shutdown function (0: shutdown mode, 1: operating mode). If SSD=0, no current is supplied to the analog circuit, GP2AP002S00F ceases its operation. See 1-5 for more detail.
VCON : Vout terminal output method control (0: normal mode, 1: interrupt mode). See 1-4 for more detail.
ASD : Select switch for analog sleep function (0: ineffective, 1: effective). See 1-8 for more detail.
OCON[1:0] : Select switches for enabling/disabling Vout terminal (00: enable, 11: force to go High, 10: force to go Low). By disabling Vout terminal, the output voltage is forced to go "H"or"L", but it does not mean the terminal getsinto high-impedance state. By enabling Vout terminal, it normally operates according to the VCON setting and the VO value. See【2】for more details on how to use this function.

1-4 Sensing Result and Output Method

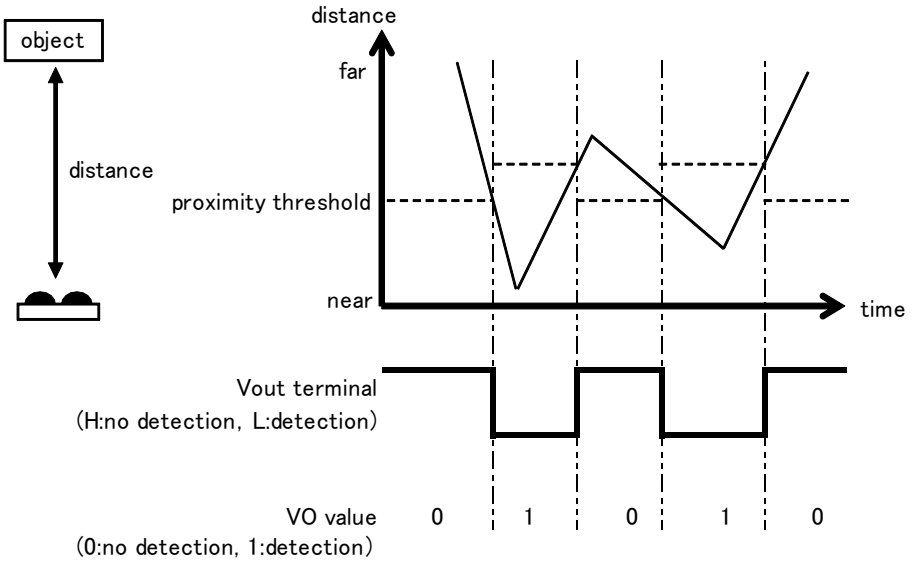
1-4-1 Sensing Result

Proximity sensing result is always accessible as VO bit in PROX register (ADDRESS 00H) through I^2C data bus (0: no object detected, 1: object detected). Normally, GP2AP002S00F updates the VO value in every fundamental detection period (~8ms) based on its original algorithm to cope with modulated light noise, in conjunction with a proper detection distance hysteresis.
As described just below, when in Vout normal output mode, GP2AP002S00F buffers VO value to Vout terminal, too. On the other hand, in Vout interrupt mode, GP2AP002S00F makes Vout terminal's operation change to create interrupt trigger signal and differently updates VO value although the internal detection circuit and algorithm are the same. The latter output method (interrupt mode) is useful in a host system in which periodic polling to read the VO value is not desirable.

1-4-2 Vout Terminal Output Method

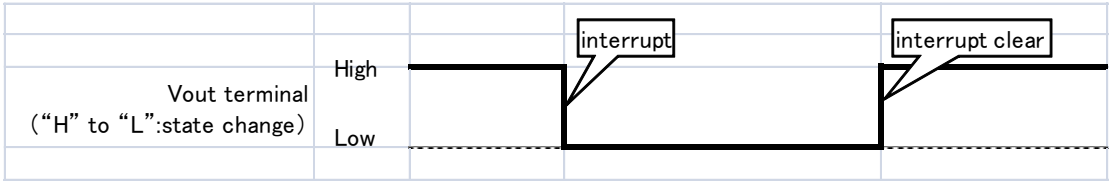
1-4-2-1 Normal Output Mode

When register OPMOD (ADDRESS 04H), VCON bit is set to "0", GP2AP002S00F operates in normal output mode. Vout terminal outputs "L" or "H" when reflective object is detected or not, respectively. Namely, the proximity sensing result, VO value, is also derived at Vout terminal in negative logic through CMOS output buffer.

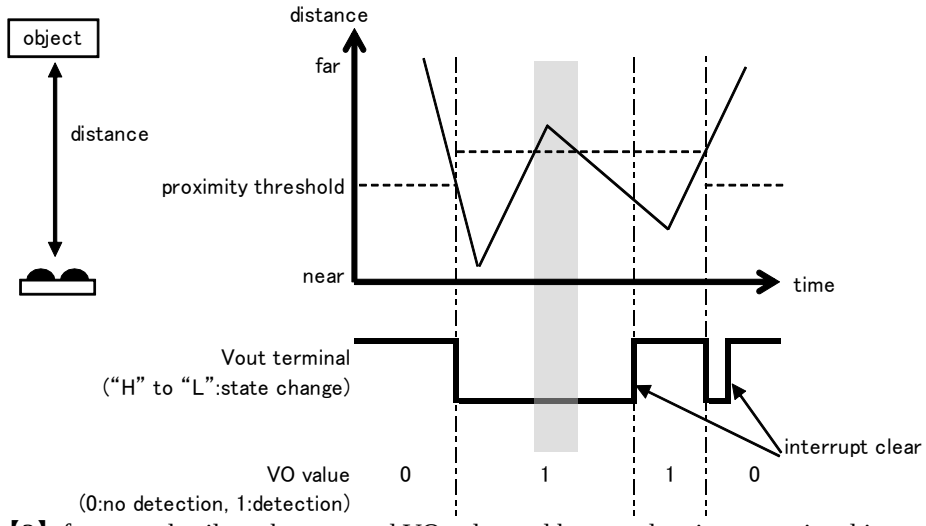


1-4-2-2 Interrupt Mode

When register OPMOD (ADDRESS 04H), VCON bit is set to “1”, GP2AP002S00F operates in interrupt mode. Vout terminal makes a transition from “H” to “L” immediately after a sensing result has been changed in either case: VO: from 0 to 1, or from 1 to 0. After making an interrupt, the Vout terminal remains at “L” level and also the GP2AP002S00F’s internal state machine ceases its operation, therefore the VO value is kept as the interrupt occurred.



For example, as shown in the figure below, after the 1st interrupt transition, although the reflective object once goes away beyond the detection threshold and gets back closer again, the VO value is still maintained as “1” (grayed area). While the Vout terminal is kept Low, GP2AP002S00F’s internal analog parts are active, but its state machine ceases sensing operation until IntClear bit is flagged to 1. Then, after restarting the sensing operation, if a newly derived sensing result differs from the previously one, GP2AP002S00F generates another interrupt signal again. In such a way, the VO value can be read out at any time convenient to the host system as accurately as in the normal output mode operation .



See also【2】for more details on how to read VO value and how to clear interrupt signal in actual situation.

1-5 Software Shutdown

Register OPMOD (ADDRESS 04H), SSD bit switches over: 1: operating mode, 0 : shutdown mode. In shutdown mode, no current is supplied to the analog circuit, GP2AP002S00F ceases its operation.
Going shutdown under Vout Normal output mode operation, use following 04H address data:

OPMOD register（ADDRESS 04H）		
d'000	b'00000000	h'00

Going shutdown under Vout interrupt mode operation, use following 04H address data:

OPMOD register（ADDRESS 04H）		
d'002	b'00000010	h'02

When Vcc power supply is turned on, GP2AP002S00F starts up in shutdown mode. The initial value of VO bit is always 0 (no detection). Regardless of SSD bit value, the register settings once written are maintained until Vcc power supply is turned off.
However, the sensing result, VO bit, is reset to 0 when SSD bit goes up to 1. Also, before going into shutdown mode, GP2AP002S00F surely turns off its LED driver circuit.
In the interrupt mode, Vout terminal stays normally “H”, and then taking “H”or“L” depending on theproximity of the object. When going shutdown, Vout terminal is immediately forced to go “H” regardless of the previous output level, Therefore, it is recommended that the host system of GP2AP002S00F should forbid interrupt input signal before issuing shutdown command to GP2AP002S00F. In addition, when going back to operating mode, the host system should permit interrupt input signal after necessary register settings are made. See【2】for more detail.

1-6 Sensitivity and Detection Distance Hysteresis Adjustment

GP2AP002S00F prevents its sensing result from chattering due to internal random noise at any detection distance. This can be done by adopting internal detection threshold levels according to the VO value. Characteristics of the detection distance and its hysteresis can be set by choosing HYSD, HYSC and HYSF registers properly. In【2】, recommended operation mode / register setting procedure, three kinds of operation mode are explained as typical combinations of these register settings. Following are brief explanations for HYS register setting.

For recommended operation mode A:

HYSD=1, HYSC[1:0]= 10, HYSF[3:0]= 0010

HYS register（ADDRESS 02H）		
d'194	b'11000010	h'C2

HYSD=1 setting enables automatic threshold control according to the VO value.

For recommended operation mode B1:

According to the derived VO value , two kinds of HYS register setting are to be used:

When VO=0 HYSD=0, HYSC[1:0]= 10, HYSF[3:0]= 0000

HYS register（ADDRESS 02H）		
d'064	b'01000000	h'40

When VO=1 HYSD=0, HYSC[1:0]= 01, HYSF[3:0]= 0000

HYS register（ADDRESS 02H）		
d'032	b'00100000	h'20

By setting HYSD=0 (disabling the automatic threshold control function), higher sensitivity and laeger hysteres than the operating mode A are available.

For recommended operation mode B2:

According to the derived VO value , two kinds of HYS register setting are to be used:

When VO=0 HYSD=0, HYSC[1:0]= 01, HYSF[3:0]= 0000

HYS register（ADDRESS 02H）		
d'032	b'00100000	h'20

When VO=1 HYSD=0, HYSC[1:0]= 00, HYSF[3:0]= 0000

HYS register（ADDRESS 02H）		
d'000	b'00000000	h'00

By setting HYSD=0 (disabling the automatic threshold control function), higher sensitivity and larger hysteres than the operating mode A are available can be targeted. The internal receiver sensitivity is now 2 times higher than in the operation mode B1.

Note that, however, the higher the sensitivity, the poorer the immunity against external noises such as power supply noise and fluorescent light noise etc. Care must be taken to make sure that the actual electrical/optical implementation affords to choose this option.

1-7 Detection Cycle

The detection cycle of GP2AP002S00F can be extended from 1x of fundamental detection period (typically ~8ms) to 128x, which is about 1 second long, by using CYCLE register (Address 03H), CYCL[2:0] bits. Extending the detection cycle helps reduce average current consumption. It is also helpful for a host system when the update cycle is too fast. The register settings to choose the detection cycle extension factor, N, are summarized below.

CYCL[2:0]			CYCLE register（ADDRESS 03H）（OSC[2]=1）			detection cycle extension factor, N	response time
d'0	b'000	h'00	d'004	b'00000100	h'04	2^0=1	8ms
d'1	b'001	h'01	d'012	b'00001100	h'0C	2^1=2	16ms
d'2	b'010	h'02	d'020	b'00010100	h'14	2^2=4	32ms
d'3	b'011	h'03	d'028	b'00011100	h'1C	2^3=8	64ms
d'4	b'100	h'04	d'036	b'00100100	h'24	2^4=16	128ms
d'5	b'101	h'05	d'044	b'00101100	h'2C	2^5=32	256ms
d'6	b'110	h'06	d'052	b'00110100	h'34	2^6=64	512ms
d'7	b'111	h'07	d'060	b'00111100	h'3C	2^7=128	1024ms

1-8 Analog Sleep Function

Register OPMOD (ADDRESS 04H), ASD bit determines if analog sleep function: 0: ineffective, 1: effective. By setting ASD=1, GP2AP002S00F de-activates internal analog circuit intermittently and partly. Analog sleep function helps minimize average operating power consumption. However, its operation is affected by stability of Vcc line. Make sure validity of usage of this function under realistic environment and conditions.

Considering the following register bits,
SSD (0: shutdown mode, 1: operating mode)
VCON (0: Vout normal output mode, 1: Vout interrupt output mode)
ASD (0: disable, 1: enable)

When setting SSD=1,VCON=0,ASD=0, use 04H register data listed below:

OPMOD register（ADDRESS 04H）		
d'001	b'00000001	h'01

When setting SSD=1,VCON=1,ASD=0, use 04H register data listed below

OPMOD register（ADDRESS 04H）		
d'003	b'00000011	h'03

When setting SSD=1,VCON=0,ASD=1, use 04H register data listed below:

OPMOD register（ADDRESS 04H）		
d'017	b'00010001	h'11

When setting SSD=1,VCON=1,ASD=1, use 04H register data listed below

OPMOD register（ADDRESS 04H）		
d'019	b'00010011	h'13

1-9 On the Average Current Consumption

Average current consumption of GP2AP002S00F is the sum of the ones through Vcc and VLED terminals.

1-9-1 Average current consumption through Vcc terminal

This is prescribed and specified in spec 3-3. Analog sleep function effectively reduces Vcc average current consumption to 1/3 times that of the corresponding specification in 3-3 (without analog sleep function). In conjunction with analog sleep function, the longer the detection cycle, the smaller Vcc average current consumption a little more . See【3】for. more detail

1-9-2 Average current consumption through VLED terminal

The longer the detection cycle, the smaller VLED average current consumption linearly.
VLED average current consumption can be estimated as follows:
[average current consumption through VLED] = [LED peak current (ILED)] x [Duty] x [1/N]

[LED peak current (ILED)] depends on external LED current limiting resistor value , R_{LED}.
Recommended ILED value is in a range of up to 170mA (See【2】).
[Duty] = 0.3%
By GP2AP002S00F's detection algorithm, the maximum value of [Duty] is 0.3% (See 1-1).
[N] = cycle extension factor (See 1-7)
For example,
[average current consumption in VLED] = 170mA x 0.3% x [1/16] (detection cycle 128ms) = 32uA

1-10 On the Countermeasure against External Light Noise

External light noise sources, which may disturb GP2AP002S00F's proper operation, include sunlight and artificial illuminations. As there are various types of amplitude modulation among illumination light sources, it is rather difficult to provide full and/or strict explanations. However, with brief classification of these noise sources, the corresponding countermeasures built in GP2AP002S00F are described as follows.

DC light: Light noises whose amplitude (intensity) is not modulated, e.g. sunlight.
AC light 1: Light noises whose amplitude (intensity) is modulated at relatively low frequencies related to commercial power lines, e.g. incandescent light or legacy fluorescent light.
AC light 2: Light noises whose amplitude (intensity) is not only modulated at relatively low frequencies related to commercial power lines, but also modulated at higher frequencies, e.g. fluorescent light driven by inverter.

For these light noise sources, GP2AP002S00F's operation is not guaranteed when one or more of them impinge(s) on a built-in photo-detector such that their amplitude (intensity) exceeds the specification (3-3 maximum acceptable illuminance, Ev) or beyond presumption of the specification. However, GP2AP002S00F is designed to work well under ordinary indoor or even outdoor circumstances by the following two countermeasures.

1-10-1 Up to presumptive level

DC light: Receiver circuit is AC-coupled, designed to GP2AP002S00F's own IR pulse.
DC light immunity should be referred to 3-3 maximum acceptable illuminance, Ev.

AC light 1: Receiver circuit is AC-coupled, designed to GP2AP002S00F's own IR pulse.
AC-light-1 immunity should be in the same range of 3-3 maximum acceptable illuminance, Ev.

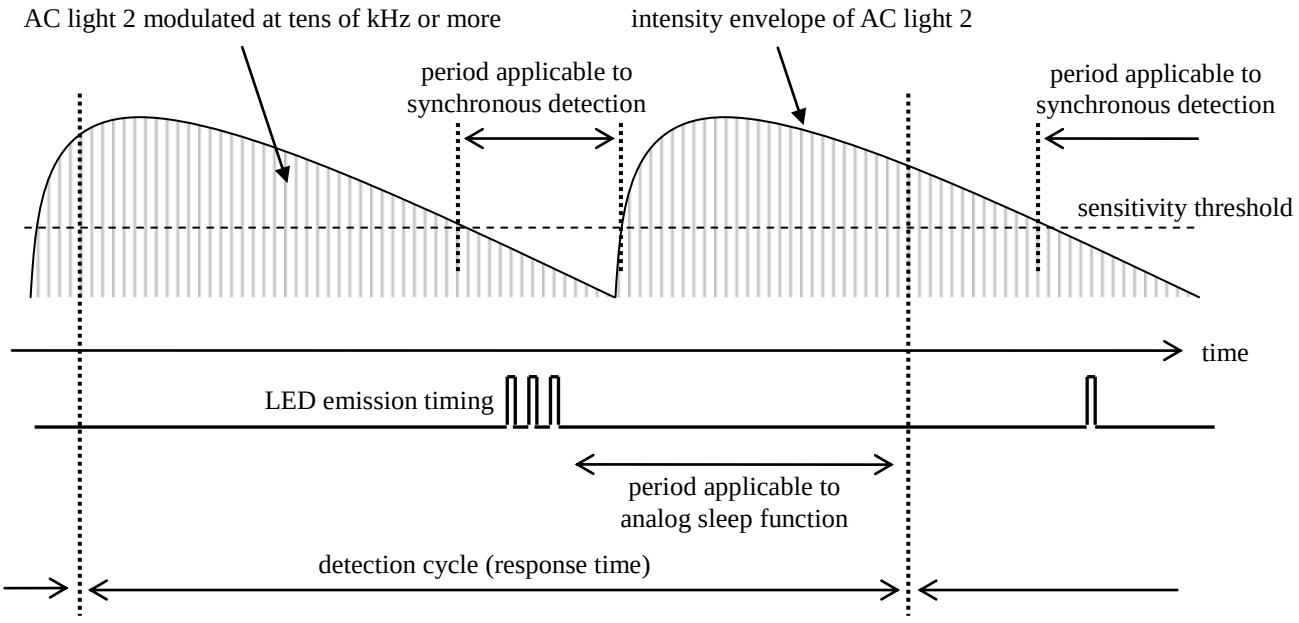
AC light 2: GP2AP002S00F tries to find proper time period to initiate its detection sequence as described below.
AC-light-2 immunity should cover ordinary indoor environment at office or home.

1-10-2 Beyond presumptive level

Regardless of the above noise source classification, if GP2AP002S00F detects their amplitude (intensity) exceeds the presumptive level, GP2AP002S00F immediately reset the VO value to 0 (no detection) in every detection cycle.

<GP2AP002S00F's operation under AC light 2>

In the figure shown below, hatched area indicates time variation of AC light 2 intensity. The envelope of the modulated intensity is periodically getting larger and smaller than a sensitivity threshold level. Obviously, GP2AP002S00F cannot make any kinds of IR LED pulse detection as long as the envelope level is larger than the threshold. In such a case, GP2AP002S00F makes successive "asynchronous" detections (without LED emission), and continues to search for a moment to initiate "synchronous" detections (with LED emission) until the envelope gets smaller than the threshold level.



<Malfunction due to unexpected strong AC light 2>

In spite of the above-mentioned countermeasure against AC light 2, under a very particular situation described below, it can happen that GP2AP002S00F falls into unwanted state, e.g. the proximity sensing result is locked to "1" (object detection). In case that a sort of locking happens, it can be reset to initial state by once letting GP2AP002S00F go shutdown and then activating it again.

【2】Recommended Operation Mode / Resister Setting Procedure

2-1 Abstract

For the purpose of detecting movement of the human body, operation of GP2AP002S00F can be optimized in terms of the following three aspects.

1. detection distance
2. detection distance hysteresis
3. response time (time interval to update the proximity sensing result)

As basic combinations, the following three operation modes are recommended.

Recommended operation mode A: with a little detection distance hysteresis

Parameter	spec.	condition	recommended circuit
1. maximum detection distance	typ.57mm	I_{LED}=170mA Needs initial register settings only	V_{CC}=3.3V , V_{LED}=3.3V , R_{LED}=6.8Ω
2. detection distance hysteresis	about 5%		
3. response time	8ms		

Recommended operation mode B1: with larger detection distance hysteresis

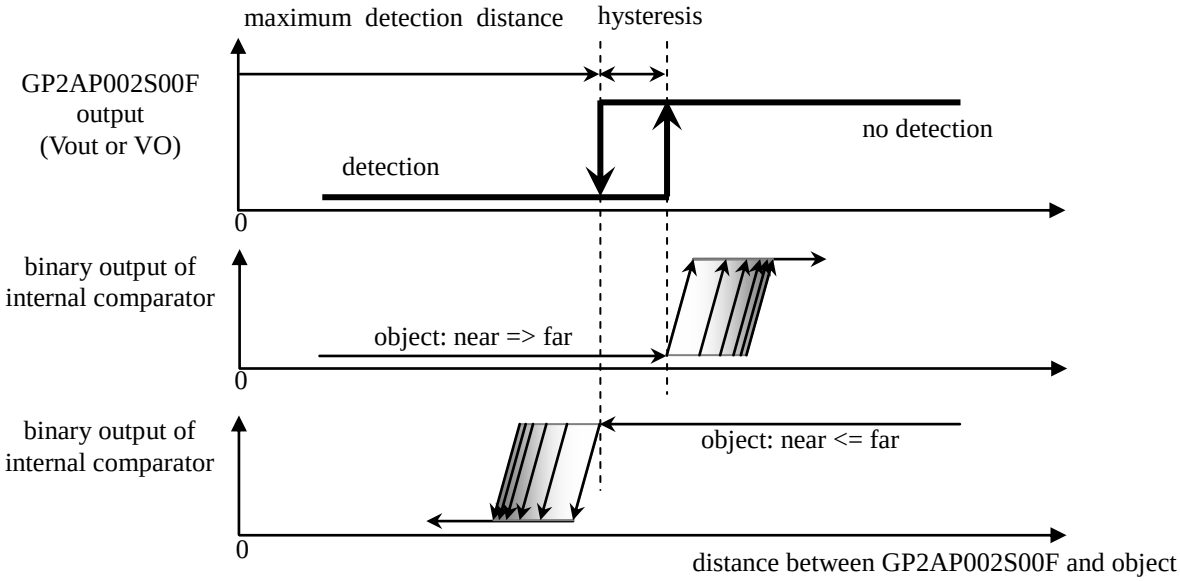
Parameter	spec.	condition	recommended circuit
1. Maximum detection distance	typ.65mm	I_{LED}=170mA Needs register settings at every interrupt output	V_{CC}=3.3V , V_{LED}=3.3V , R_{LED}=6.8Ω
2. detection distance Hysteresis	about 20%		
3. response time	8ms		

Recommended operation mode B2: with larger detection distance hysteresis, 2x higher sensitivity than B1

Parameter	spec.	condition	recommended circuit
1. Maximum detection distance	typ.65mm	I_{LED}=85mA Needs register settings at every interrupt output	V_{CC}=3.3V , V_{LED}=3.3V , R_{LED}=20Ω
2. detection distance hysteresis	about 10%		
3. response time	8ms		

Definition of the maximum detection distance and detection distance hysteresis

Detection distance hysteresis
= hysteresis / maximum detection distance



Note that the detection distance can be controlled by changing LED current limiting resistor, too.

2-2 Recommended Operation Mode A

Recommended operation A assumes Vout normal output (VCON=0) and 02H HYS register's HYSD=1. This combination leads to GP2AP002S00F's automatic, continuous operation after its initialization procedure. However, compared with recommended operation mode B in 2-3, the mode A can only provide relatively shorter detection distances and less flexibility to expand detection distance hysteresis while keeping the same detection distance. In the Vout normal output mode, IntClear bit is ineffective (disregarded).

2-2-1 Initiate operation

Procedure 1 : After power supply is turned on, set up the following registers. The other bits not shown here in the listed address should be set to 0.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
01H	GAIN	LED[0]	b'1	d'008	b'00001000	h'08	in any order
02H	HYS	HYSD	b'1	d'194	b'11000010	h'C2	
		HYSC[1:0]	b'10				
		HYSF[3:0]	b'0010				
03H	CYCLE	CYCL[2:0]	b'000	d'004	b'00000100	h'04	
		OSC[2]	b'1				
04H	OPMOD	SSD	b'1	d'003	b'00000001	h'01	after HYS register setup
		VCON	b'0				

Note : To extend the detection cycle from fundamental period (~8ms), see 1-7. To use Analog Sleep function, see 1-8.

Procedure 2 : Acquire proximity sensing results by reading Vout directly or VO bit through I^2C bus interface.

2-2-2 Software shutdown, and Go back to operation in the normal output mode

To go shutdown (SSD:1=>0) under the normal output mode operation, use 04H address data shown below.

register ADDRESS	register SYMBOL	register BIT	WRITE Value				remarks
			BIT data	ADDRESS data			
04H	OPMOD	SSD	b'0	d'000	b'00000000	h'00	
		VCON	b'0				

To go back to operation (SSD:0=>1), use 04H address data shown below.

register ADDRESS	register SYMBOL	register BIT	WRITE Value				remarks
			BIT data	ADDRESS data			
04H	OPMOD	SSD	b'1	d'001	b'00000001	h'01	
		VCON	b'0				

When it is necessary to keep Vout terminal "H" through entire shutdown period, the register CON (address 06H) is available. Set CON[4:3] bits according to the following procedures. Note that the CON[4:3] settings disable Vout output, however, which means Vout terminal forced to go "H" or "L" state and does not mean to get high impedance state.

Procedure 1 : Set 06H CON register as follows, forcing Vout terminal to go "H".

register ADDRESS	register SYMBOL	register BIT	WRITE Value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'11	d'024	b'00011000	h'18	

Procedure 2 : Release from shutdown.

register ADDRESS	register SYMBOL	register BIT	WRITE Value				remarks
			BIT data	ADDRESS data			
04H	OPMOD	SSD	b'1	d'001	b'00000001	h'01	
		VCON	b'0				

Procedure 3 : Set 06H CON register as follows, enabling Vout terminal in normal operation.

register ADDRESS	register SYMBOL	register BIT	WRITE Value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'00	d'000	b'00000000	h'00	

Procedure 4 : Acquire proximity sensing results by reading Vout directly or VO bit through I^2C bus interface.

2-3 Recommended Operation Mode B

(Procedures shown below correspond to operation mode B1. The only difference in register settings between B1 and B2 is HYSC[1:0] setting. See 1-6.)

Provided that GP2AP002S00F operate in the interrupt mode (VCON=1), operation mode B's can target relatively longer detection distance and larger detection distance hysteresis, compared with operation mode A, by setting HYS register according to the derived VO value.

In accordance with the following procedures in 2-3-1 and 2-3-2, GP2AP002S00F can be dealt by host systems which may differ from each other in terms of signal processing when interrupt signal comes in: level-sense type or edge-triggered type. To this end, in addition to the VO-dependent 02H HYS register setting, it is also necessary to set up 06H CON register's CON[4:3] bits. Note that the CON[4:3] settings disable Vout output, however, which means Vout terminal forced to go "H" or "L" state and does not mean to get high impedance state.

2-3-1 When the read format Acceptable

The following procedures in 2-3-1-1 and 2-3-1-2 are applicable when a host system is able to write arbitrarily from master to slave in the 2nd byte (after the 1st byte transmission of the slave address with read request) of the three-byte read format described in 1-2-2, that is, IntClear bit of the 2nd byte's MSB can be set to either 1 (SDA: H) or 0 (SDA: L).

On the other hand, for a host system that can only makes a dummy read for the 2nd byte, that is, IntClear bit is no other than 1 (SDA: H) by doing so, consider implementing the other procedures described in 2-3-2.

2-3-1-1 Initiate operation

Procedure 1 : After power supply is turned on, set up the following registers. The other bits not shown here in the listed address should be set to 0.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
01H	GAIN	LED[0]	b'1	d'008	b'00001000	h'08	in any order
02H	HYS	HYSD	b'0	d'064	b'01000000	h'40	
		HYSC[1:0]	b'10				
		HYSF[3:0]	b'0000				
03H	CYCLE	CYCL[2:0]	b'000	d'004	b'00000100	h'04	
		OSC[2]	b'1				
04H	OPMOD	SSD	b'1	d'003	b'00000011	h'03	after HYS register setup
		VCON	b'1				

Note : To extend the detection cycle from fundamental period (~8ms), see 1-7. To use Analog Sleep function, see 1-8.

Procedure 2 : Permit host's interrupt input.

Procedure 3 : Vout terminal changes from "H" to "L".

Procedure 4 : Forbid host's interrupt input.

Procedure 5 : Read VO value through I^2C bus interface . VO=0: no detection, VO=1: detection
In this read transaction, IntClear bit must be "0" (i.e., Do not clear the interruption). If it is difficult for a host system to issue such a transaction, see 2-3-2 for the other procedures to avoid this difficulty.

Procedure 6 : According to the VO value derived at Procedure 5,write HYS register through I^2C bus interface: if VO=0, HYSD=0, HYSC[1:0]= 10, HYSF[3:0]= 0000 (as Procedure 1)

register ADDRESS	Register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
02H	HYS	HYSD	b'0	d'064	b'01000000	h'40	IntClear=0
		HYSC[1:0]	b'10				
		HYSF[3:0]	b'0000				

if VO=1, HYSD=0, HYSC[1:0]= 01, HYSF[3:0]= 0000

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
02H	HYS	HYSD	b'0	d'032	b'00100000	h'20	IntClear=0
		HYSC[1:0]	b'01				
		HYSF[3:0]	b'0000				

Procedure 7 : Set 06H CON register as follows, forcing Vout terminal to go "H".

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'11	d'024	b'00011000	h'18	IntClear=0

Procedure 8 : Permit host's interrupt input.

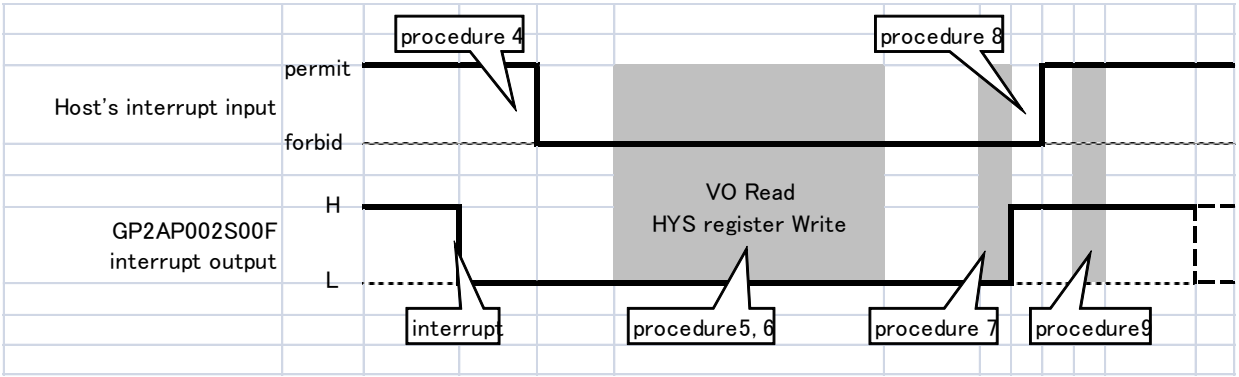
Procedure 9 : Set 06H CON register as follows, enabling Vout terminal in normal operation.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'00	d'000	b'00000000	h'00	IntClear=1

Procedure 10 : Repeat procedures from 3 to 9.

Note the remarked IntClear setting in each procedure. These procedures prevent a host system from being exposed to potential erroneous detection by changing IntClear bit from 0 to 1 after the necessary settings have been made.

The following figure shows relationship between host's interrupt reception and behavior of GP2AP002S00F's Vout terminal described above.



2-3-1-2 Software shutdown, and Go back to operation in the interrupt output mode

To go shutdown (SSD:1=>0) under the interrupt mode operation, use 04H address data shown below.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
04H	OPMOD	SSD	b'0	d'002	b'00000010	h'02	
		VCON	b'1				

Note that this setup should be done after host's interrupt is made forbidden.

To go back to operation (SSD:0=>1), follow the procedures below.

Procedure 1: Set 06H CON register as follows, forcing Vout terminal to go "H".

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'11	d'024	b'00011000	h'18	IntClear=0

Procedure 2: Set 02H HYS register as follows, preparing VO reset to 0.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
02H	HYS	HYSD	b'0	d'064	b'11000010	h'40	IntClear=0
		HYSC[1:0]	b'10				
		HYSF[3:0]	b'0000				

Procedure 3: Release from shutdown.

register ADDRESS	register SYMBOL	register BIT	WRITE value BIT data	WRITE value ADDRESS data			remarks
04H	OPMOD	SSD	b'1	d'003	b'00000011	h'03	IntClear=0
		VCON	b'1				

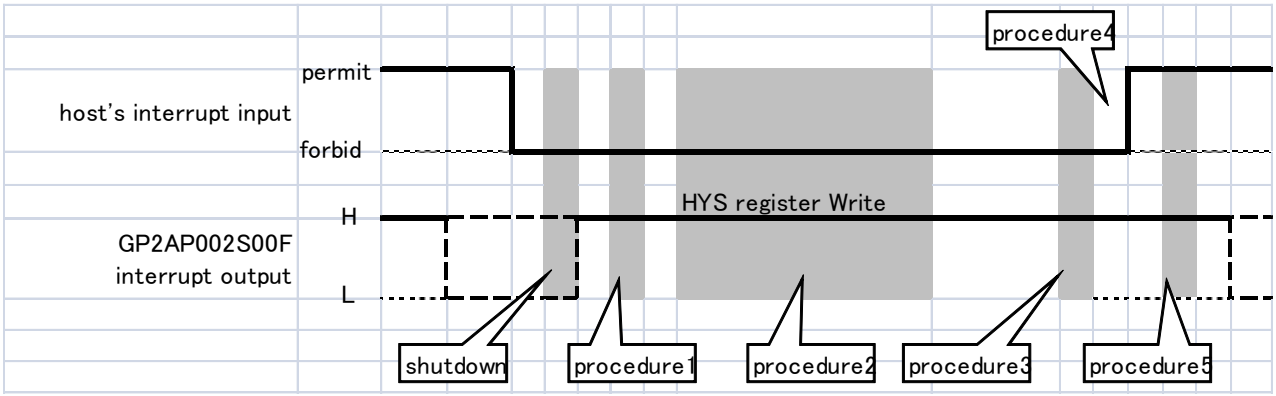
Procedure 4: Permit host's interrupt input

Procedure 5: Set 06H CON register as follows, enabling Vout terminal in normal interrupt operation.

register ADDRESS	register SYMBOL	register BIT	WRITE value BIT data	WRITE value ADDRESS data			remarks
06H	CON	OCON[1:0]	b'00	d'000	b'00000000	h'00	IntClear=0

Note that the IntClear settings are changed from initiation process 2-3-1-1.

The following figure shows relationship between host's interrupt reception and behavior of GP2AP002S00F's Vout terminal described above.



2-3-2 When the read format Unacceptable

The following procedure in 2-3-2-1 are recommended to use when a host system is not able to write arbitrarily from master to slave in the 2nd byte of the three-byte read format as described in 1-2-2, that is, the host system is not able to pull down the SDA line (i.e., IntClear=0) in the read transaction.

Differences between the procedures described here and those in 2-3-1 are summarized below. First, the host system should have its own variable for proximity sensing result, e.g. MVO (master's VO), as GP2AP002S00F has its own VO value. Also, the host system should update the MVO value by counting GP2AP002S00F's interrupt signal generation instead of referring to the VO value. Then, HYS and the other register settings are made according to the current MVO value. In the last part of the procedures, the VO value is finally read out and compared with the MVO value in order to check if the both values correspond. In this way, the following procedure prevent a host system from being exposed to potential erroneous detection, as well as the procedures in 2-3-1 do, by letting IntClear bit be 1 after the necessary settings have been made. If MVO and VO values do not correspond, they should be initialized (reset to 0 : no detection) at the same time. The VO value can be reset by letting GP2AP002S00F go shutdown and re-activating it again.

2-3-2-1 Initiate operation

Procedure 1 : After power supply is turned on, set up the following registers. The other bits not shown here in the listed address should be set to 0.

register ADDRESS	register SYMBOL	register BIT	WRITE value BIT data	WRITE value ADDRESS data			remarks
01H	GAIN	LED[0]	b'1	d'008	b'00001000	h'08	in any order
02H	HYS	HYSD	b'0	d'064	b'01000000	h'40	
		HYSC[1:0]	b'10				
		HYSF[3:0]	b'0000				
03H	CYCLE	CYCL[2:0]	b'000	d'004	b'00000100	h'04	
		OSC[2]	b'1				
04H	OPMOD	SSD	b'1	d'003	b'00000011	h'03	after HYS register setup
		VCON	b'1				

Note 1: To extend the detection cycle from fundamental period (~8ms), see 1-7. To use Analog Sleep function, see 1-8.

Note 2: The VO value is always 0 (no detection) after this procedure, so the MVO value should also be initialized to 0.

Procedure 2 : Permit host's interrupt input.

Procedure 3 : Vout terminal changes from "H" to "L".
At this moment, do not read the VO value (i.e., Do not clear the interruption). Instead, update the MVO value (master's VO value) as follows. By counting the interrupt transitions from Procedure 1 throughout the entire operation, the host system should recognize that at odd-numbered interruptions, including the 1st one here, the VO value has changed from 0 to 1, and at even-numbered interruptions, from 1 to 0, respectively.

Procedure 4 : Forbid host's interrupt input.

Procedure 5 : According to the MVO value derived at procedure 3, write HYS register through I^2C bus interface as follows:

if VO=0, HYSD=0, HYSC[1:0]= 10, HYSF[3:0]= 0000 (as Procedure 1)

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
02H	HYS	HYSD	b'0	d'064	b'01000000	h'40	IntClear=0
		HYSC[1:0]	b'10				
		HYSF[3:0]	b'0000				

if VO=1, HYSD=0, HYSC[1:0]= 01, HYSF[3:0]= 0000

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
02H	HYS	HYSD	B'0	d'032	b'00100000	h'20	IntClear=0
		HYSC[1:0]	b'01				
		HYSF[3:0]	b'0000				

Procedure 6 : Set 06H CON register as follows, forcing Vout terminal to go"H".

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'11	d'024	b'00011000	h'18	IntClear=0

Procedure 7 : Read the VO value in the 3rd byte of the read format described in 1-2-2 with a dummy read for the 2nd byte (i.e., SDA is kept at H there). GP2AP002S00F regards the dummy byte's MSB as IntClear flagged to 1.
Note that, in the 2nd byte, GP2AP002S00F also ACKnowledges according to its read format until next SCL falling edge comes in.
Then, compare the MVO value and the VO value:
A) If the MVO is corresponding to the VO values, go to Procedure 8.
B) If not, it should be recognized that there is something unexpected in the device's I/O part or somewhere else in the I^2C bus interface. Therefore, it is recommended to reset GP2AP002S00F and the MVO value as follows. (However, this example of error treatments can be changed independently from the other Procedures 1 through 10 described here.)

*Set 04H OPMOD register as follows, to let GP2AP002S00F go shutdown.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
04H	OPMOD	SSD	b'0	d'002	b'00000010	h'02	IntClear=0
		VCON	b'1				

* Reset the MVO value to 0: no detection.

*Then, set 04H OPMOD register as follows to let GP2AP002S00F wake up again with the initial value of the VO bit (0: no detection).

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
04H	OPMOD	SSD	b'1	d'003	b'00000011	h'03	IntClear=0
		VCON	b'1				

*Go back to Procedure 2 (Or, if necessary, go back to Procedure1 for the register settings needed).

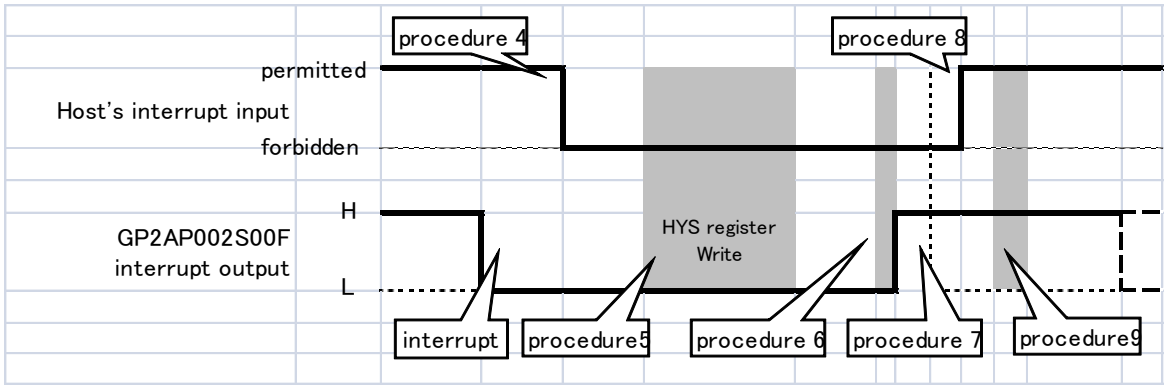
Procedure 8 : Permit host's interrupt input.
Procedure 9 : Set 06H CON register as follows, enabling Vout terminal in normal operation.

register ADDRESS	register SYMBOL	register BIT	WRITE value				remarks
			BIT data	ADDRESS data			
06H	CON	OCON[1:0]	b'00	d'000	b'00000000	h'00	IntClear=0

Procedure 10 : Repeat procedures from 3 to 9.

Note that the IntClear setting is all 0 throughout the procedures from 1 to 10.

The following figure shows relationship between host's interrupt reception and behavior of GP2AP002S00F's Vout terminal described above.

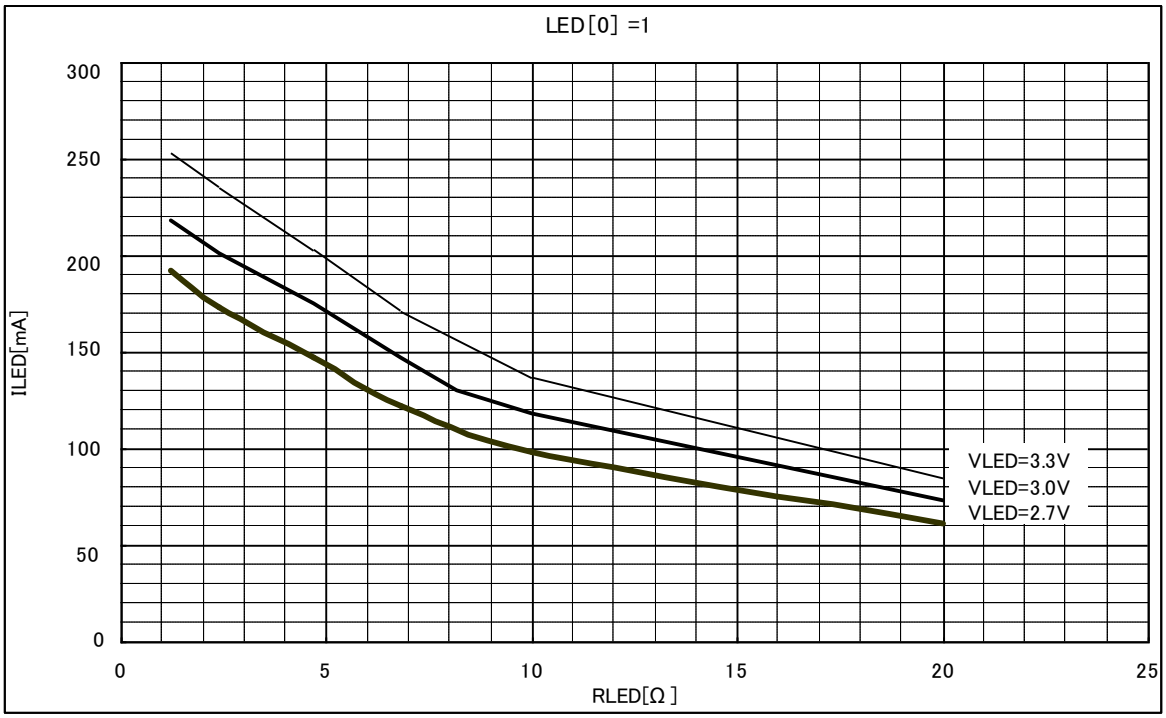


Also, with respect to going shutdown and going back to operation, the procedures are all the same as described in 2-3-1-2 because there is no use of read format.

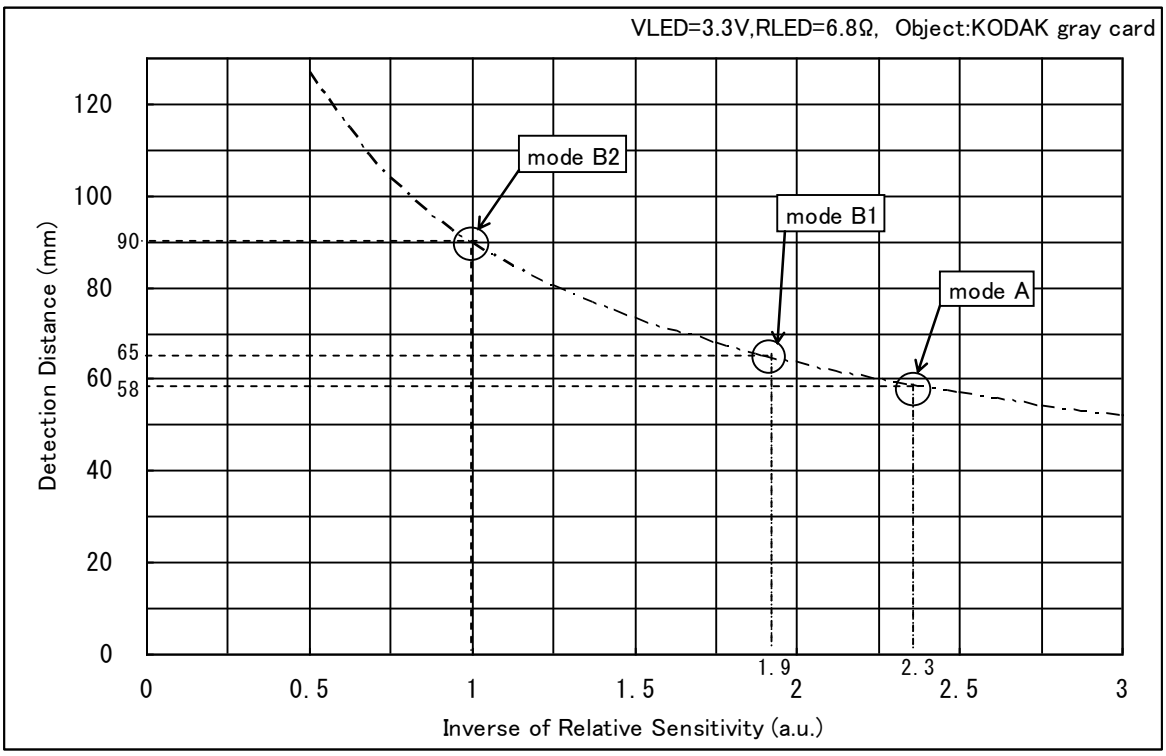
【3】Data (Reference)

3-1 I_{LED} Setting by R_{LED}

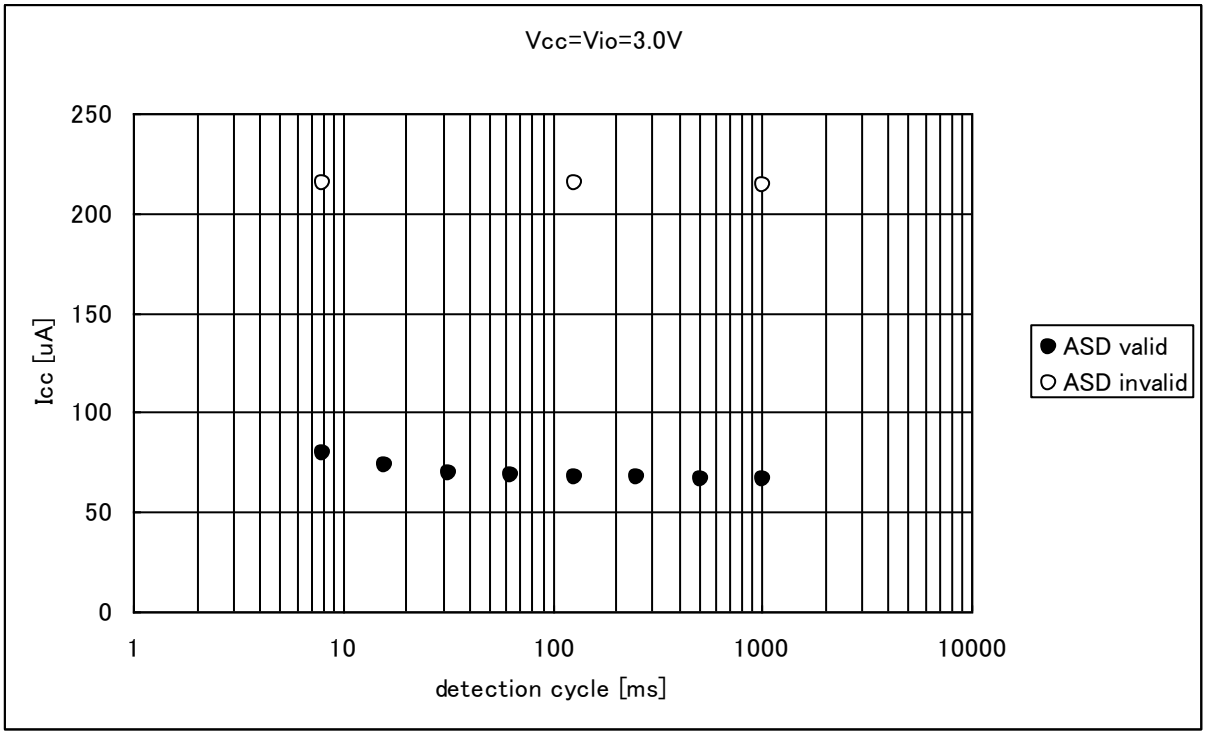
(Vcc=3.0V)



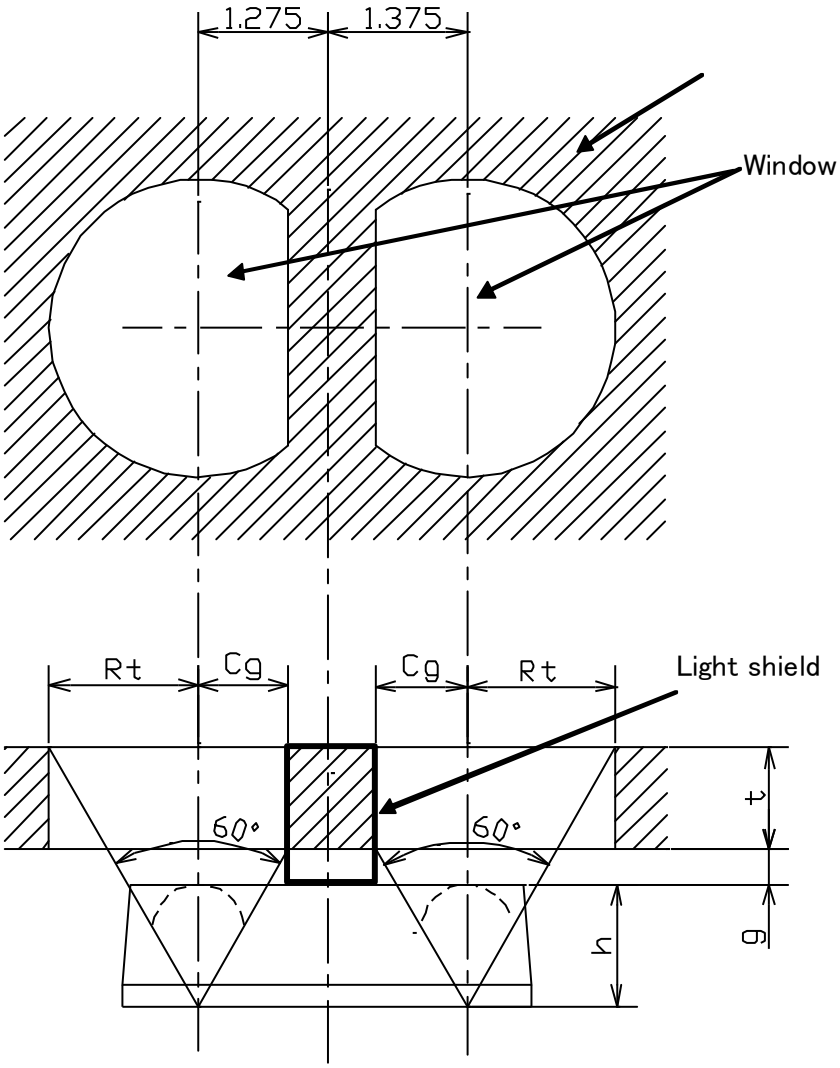
3-2 Sensitivity Setting vs Detection Distance



3-3 ICC dependence on Detection Cycle and Analog Sleep Function



【4】Recommended Window Size (Reference)



h= n×r / (n - 1) =1.2mm
n=1.58 n : mold resin refractive index
r =0.45 r : radius

Cg =(h+g)×tan30
Rt = (h+g+t)×tan30
g<0.7mm

1. The print please use ink, the paint which do not transmit infrared.
2. Please carry out printing between the window by all means,or using light shield.
3. Even recommended print size may cause false detection depending on the reflectance of the panel.
   In this case it is effective when I widen print width between the window, but affects detection distance.
4. When I_{LED}, a mode change by the same window design, malfunction may occur.
   Please confirm that I do not have any problem with an actual machine in there being a case to malfunction if I_{LED} in particular is high.
5. Please confirm a thing without the problem with an actual machine in consideration of the position gap
6. The recommended transmissivity of the filter is more than 85%. (at wavelength λ=940nm)
7. In order to reduce direct reflection from the outer window, it is recommended that an opaque abstacle be placed between the emitter and detector sides as shown in the figure.