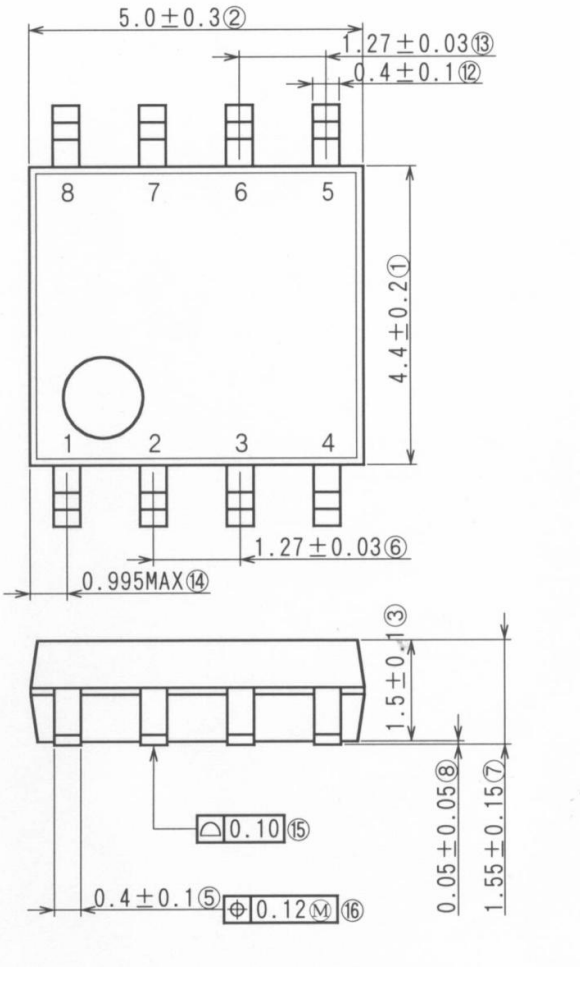
IR3M92N4
Application note

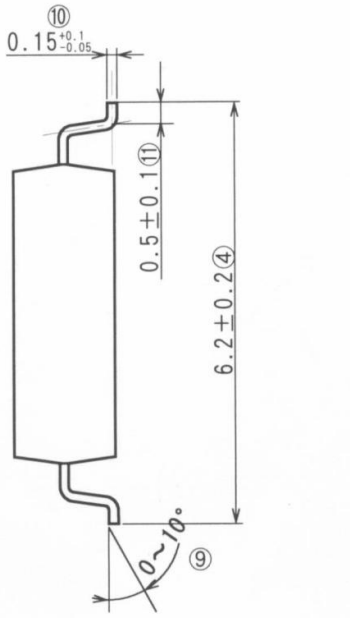
Contents

1. General description

IR3M92N4 is a controller IC of LED Lighting power supply.
Operation mode is Critical Current Mode. It can enable high power factor by controlling ON period constant, and enable high efficiency and low EMI by quasi-resonant operation.
Either insulated or non-insulated circuit is capable in accordance with the purpose.
Insulated circuit uses flyback converter method, and is able to control in high power factor and high accuracy.
Non-insulated circuit uses step up or step down converter method with transformer, and is able to control in high power factor, high accuracy and high efficiency. In comparison with insulated circuit, non-insulated circuit can smaller the size and lower the price of the power system by decreasing external components.

2. Pin assignment and Package outline





①	OUT
②	GND
③	ISE
④	VSE
⑤	FL1
⑥	FL2
⑦	FUNC
⑧	VCC

3. Pin description

Pin name	Pin description
1. OUT	Gate drive for the external switching MOSFET
2. GND	Ground pin
3. ISE	Current sense of the primary winding
4. VSE	Voltage sense of the auxiliary winding
5. FL1	The input pin of error amplifier.
6. FL2	The output pin of error amplifier.
7. FUNC	Mode detection pin
8. VCC	Power supply pin

4. Absolute maximum ratings

Absolute maximum ratings are values or ranges which can cause permanent damage.
Please do not exceed this range even when start up or shut down. Ta=25°C

Parameter	Symbol	Rating	Unit	Applied terminal
Power Supply Voltage	Vcc	-0.3 ~ 28.0	V	VCC
Input Terminal Voltage	VI1	-0.3 ~ 6.0	V	ISE, VSE, FL1,FL2,FUNC
Output Terminal Voltage	VO1	-0.3 ~ 28.0	V	OUT
Operating Temperature	TOPR	-30 ~ 100	°C	
Storage Temperature	TSTG	-40 ~ 150	°C	

5. Electrical characteristics

Unless otherwise specified, condition shall be GND=ISE=VSE=0V, VCC=12V, Ta=25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VCC section						
VCC Input Voltage	VCC1	10	12	18	V	
VCC Startup Current	ICC1	—	30	80	uA	VCC=Startup voltage - 0.1V
VCC Operating supply current	ICC2	—	1.0	2.0	mA	
VCC Turn on threshold	Vst	15.5	18.0	20.0	V	
VCC Turn off threshold	Vuvlo	5.0	6.0	7.5	V	
Gate driver section						
Output Low Resistance	RL	—	—	15	Ω	OUT - 0.1V
Output High Current	IOH	40	—	—	mA	OUT < 8V
Oscillator section						
Frequency	fosc	135	210	300	kHz	FL2=2.5V
Error Amplifier Section						
Reference Voltage	VREF	2.94	3.00	3.06	V	(※)
Feedback Voltage	VFB	873	900	927	mV	VSE=1V,ISE=0.3V,FL2=2.5V
Transconductance	Gm	—	43	—	uA/V	FL1=0.9V
FL2 Operating range	Vfl2	0.5	—	4.0	V	
Zero Cross Detect Section						
VSE Threshold Voltage	VVSE	0.2	0.3	0.4	V	FL2=2.5V
FUNC section						
Threshold Voltage of Flyback mode	VFLY	3.2	—	4.5	V	
Threshold Voltage of StepDown mode	VStepD	1.45	—	2.85	V	
Threshold Voltage of Stanby mode	Vstby	—	—	0.8	V	
Threshold High Voltage of PWM	VPWMH	1.45	—	4.50	V	
Threshold Low Voltage of PWM	VPWML	—	—	0.8	V	
FUNC Bias Current	IFUNC	8.7	10.0	12.5	uA	
Over Current Protection Section						
Threshold Voltage of Flyback	VOCP_FLY	1.45	1.60	1.75	V	FL2=2.5V
Threshold Voltage of StepDown	VOCP_StepD	0.65	0.80	0.95	V	FL2=2.5V
Minimum Off Time in OCP	tmin	40	70	120	us	
Leading edge blanking time	tleb1	—	200	—	ns	
Over Voltage Protection Section						
Threshold Voltage of VSE	VOVP_VSE	1.9	2.1	2.3	V	
Threshold Voltage of VCC	VOVP_VCC	22	23	24	V	
Leading edge blanking time	tleb2	—	600	—	ns	
Over Temperature Protection Section						
Threshold Temperature	TSD	135	150	165	°C	Junction temperature, (※)

(※) It is secured by the design and the test is not done.

6. Operation mode description

6.1 Critical Current Mode operation

When using insulated flyback converter method, this IC will operate in Critical Current Mode by detecting the timing when the secondary inductor's current becomes 0mA, and turn on the FET.
When using non-insulated step up converter, step down converter, or choke coil method, this IC will operate in Critical Current Mode by detecting the timing when the primary inductor's current becomes 0mA, and turn on the FET.

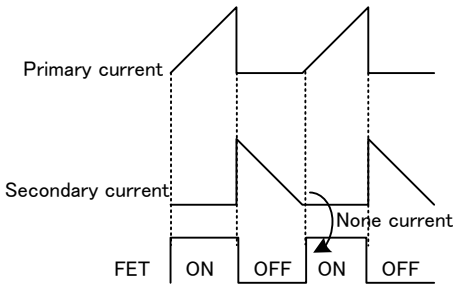


Fig.1 Critical Current Mode operation

6.2 Power factor improvement operation

ON period will become almost constant by error amplifier controlling.
Since ON period is constant, peak current of inductor will vary in proportion with input voltage.
Therefore input current varies in accordance with input voltage, and the power factor will improve.

di(t) = v(t) dt ／L* ---- Peak current of inductor is proportional with input voltage, when ON period is the same.

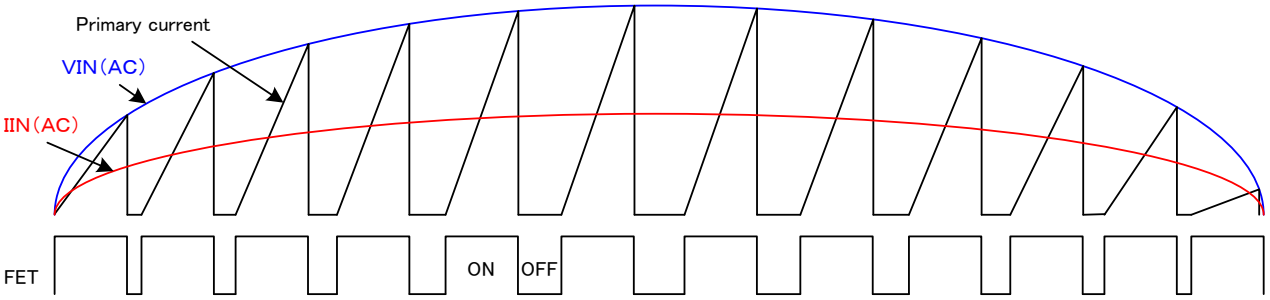


Fig.2 Improvement of power factor by constant ON time operation.

6.3 Quasi-resonant operation

This IC will drive the FET by Critical Current Mode, which detect the timing when the current of inductor becomes 0mA and turn on the FET.
When it is not Critical Current Mode, as shown in figure 3, after releasing all the energy of inductor the inductance of primary transformer and the parasitic capacitance will cause ringing at the drain of FET, and spread EMI around the circuit.
When it is Critical Current Mode, the VSE terminal monitors the timing when inductor release all the energy and turn on FET almost at the bottom point of ringing waveform, which is called quasi-resonant operation. Therefore it can minimize the noise of EMI to spread around the circuit.

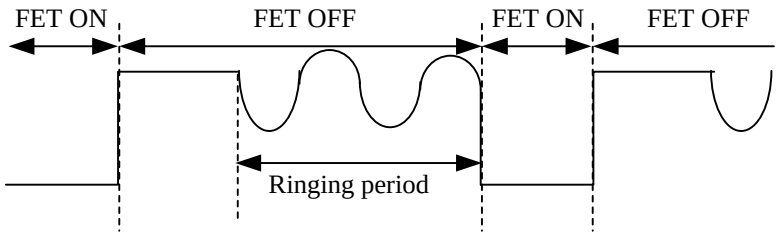


Fig.3 Waveform of FET drain (Not Critical Current Mode)

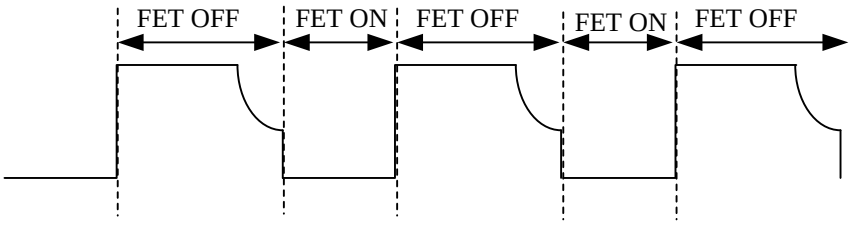


Fig.4 Waveform of FET drain (Critical Current Mode)

6.4 Constant Current Output Operation

When it is insulated flyback converter, constant current output is enabled only by using primary current control, without using feedback of secondary (LED) current by Photo coupler.
As shown in figure 4, the average amount of output current (Iout) can be expressed by using peak current of secondary current (Ipk2) and the period secondary current flows (Tres).
Iout = 1 / 2 * Ipk2 * Tres / Tc (1)
Peak current of primary and secondary current has relation with the ratio of primary and secondary winding.
Ipk2 = Np / Ns * Ipk1 (2)
(Np=primary winding turns, Ns=secondary winding turns)
Tres/Tc can be detected by using auxiliary winding which is set in primary transformer.
Iout = 1 / 2 * Np / Ns * Ipk1 * Tres / Tc (3)
Constant current output can be obtained also in non-insulated step up circuit.
In this circuit Ipk2=Ipk1, and will be expressed as shown below.
Iout = 1 / 2 * Ipk1 * Tres / Tc (4)

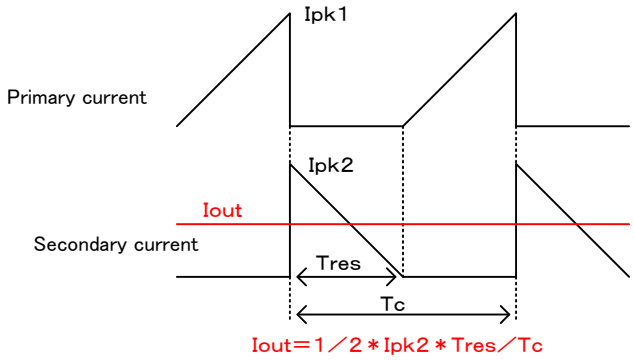


Fig.5 Constant current output control

In case of non-insulated step down method as well as step up method, Ipk2=Ipk1.
If you set Tres/Tc=1, the average amount of output current (Iout) can be expressed as below.
Please refer to figure.6
Iout = 1 / 2 * Ipk1 (5)

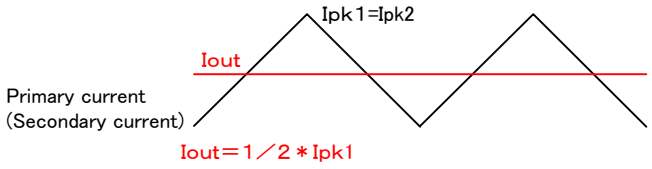


Fig.6 Constant current output control

7. Block description inside the IC

7.1 Start up circuit (VCC)

FET starts switching when VCC reaches up to start up voltage Vstart=Typ.18V.
After turning on AC voltage, current is supplied to Cvcc from VIN through Rstart, and VCC voltage rises.
Tstart, which is the time for VCC to reach start up voltage can be expressed as shown below.
Tstart = Cvcc * Vstart / (I1 - I2) (6)
I2 is current consumed in IC. I1 is current supplied from VIN through Rstart. I1 can be expressed as shown below.
I1 = (VIN - VCC) / Rstart
Equation (10) can be expressed as shown below, using the equation above.
Tstart = Cvcc * Vstart / ((VIN - VCC) / Rstart - I2) (7)
And the loss at Rstart is expressed as shown below.
Rstart Loss = (VIN - VCC) ^ 2 / Rstart (8)
When, Vstart=18V, VCC=18V, I2=30uA, C2=10uF, Rstart=300kΩ, VIN=100V
T = 10uF * 20V / ((100V - 20V) / 300kΩ - 30uA)
= 0.85s
Rstart Loss = (100 - 17.8) ^ 2 / 300kΩ
= 23mW
Rstart should be smaller to speed up start-up sequence, but it has demerit of larger loss.

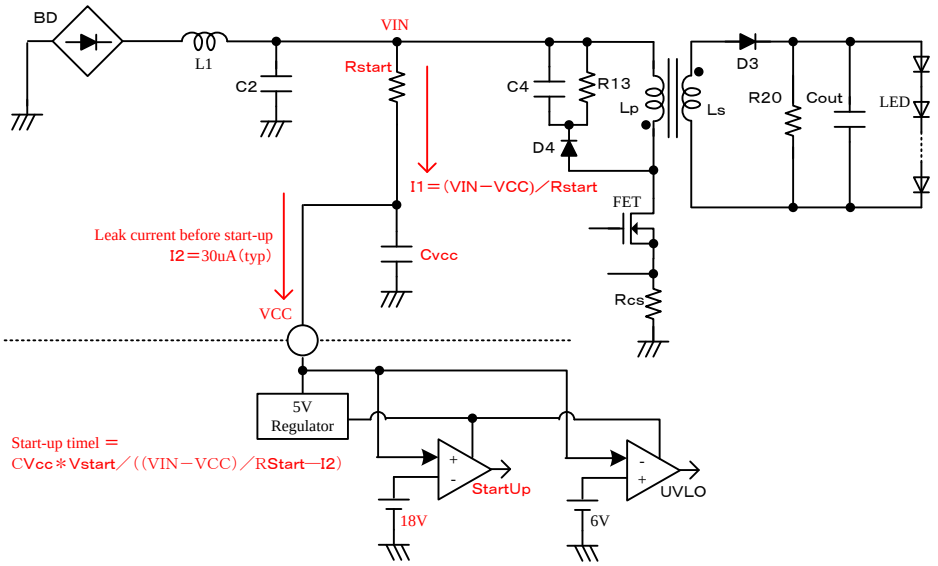


Fig.7 Start-up time

The capacitor connected to VCC must be a sufficient value, since it must keep VCC over UVLO voltage until feedback voltage from auxiliary winding (VAUX) reaches up to UVLO voltage (6V (Typ.)),

$$UVLO6V < VCC = (VAUX - VD2) = (Na / Ns) * (VLED - VD3) \quad (9)$$

where VD2 is voltage drop of diode D2, and VD3 is voltage drop of diode D3.

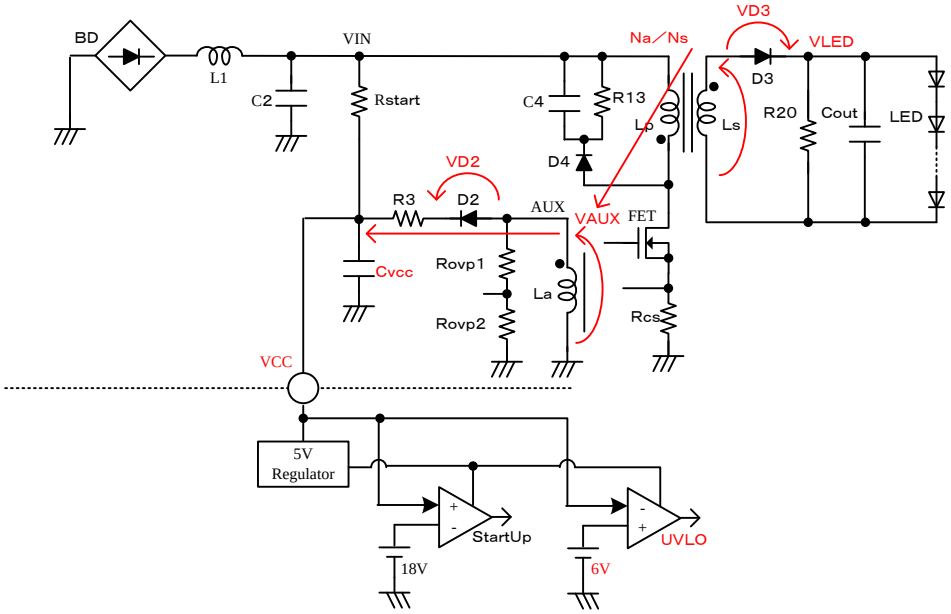


Fig.8 VCC power supply circuit from auxiliary winding

7.2 Switching circuit (OUT)

Connect the Gate of FET to OUT terminal.
When VSE goes down to 0.3V or less, FET turns on after 200ns (Typ.) delay time. The period FET is on is the sum of the time in accordance with output voltage (FL2) of error amplifier (EAMP) and 200ns (Typ.) delay time.

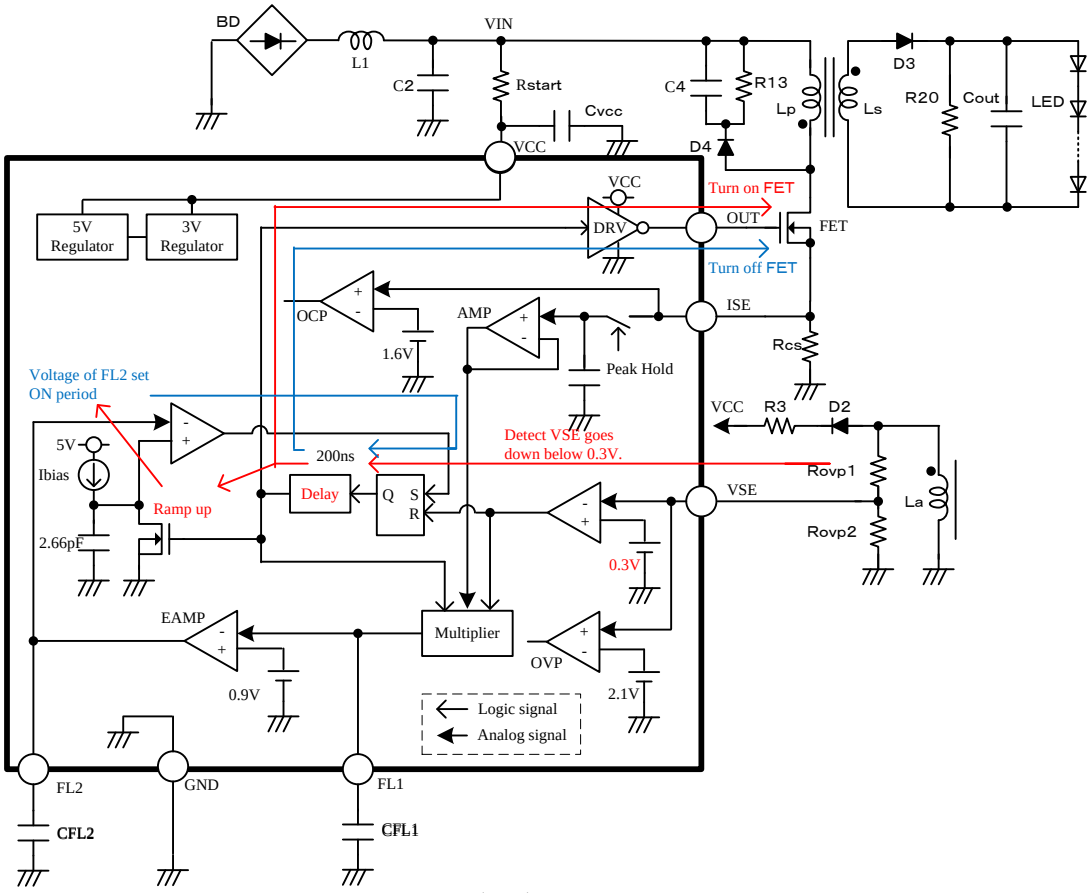


Fig.9 FET switching circuit (OUT)

FET ON timing = 200ns after VSE terminal goes down to 0.3V.
FET ON period = period in accordance with FL2 + delay time 200ns.

※The period in accordance with FL2 can be referred in “7.6 Error Amplifier (FL2)”.

7.3 ON timing detecting circuit (VSE)

When FET turns off, the drain voltage of FET rises, and voltage in accordance with the winding turns ratio arise at secondary and auxiliary windings. Since current of LED starts to flow when secondary winding voltage goes up to VLED + VD3, the voltage of auxiliary winding can be expressed as
(VLED + VD3) * Na / Np
When secondary current goes down to 0mA, the voltage of secondary winding and auxiliary winding decreases. VSE terminal has two purpose. First to detect the voltage decrease of auxiliary winding, to indicate the next ON timing. And second to measure the period that current flows at secondary winding (Tres).
When VSE goes down to 0.3V or less, after 600ns (Typ.) period of leading edge blanking from the FET OFF timing, FET turns on. Leading edge blanking period is made to mask the period until the VSE voltage stabilizes after FET off.
Actually there is error time (ΔT). After secondary winding current becomes 0mA, VSE terminal voltage starts decrease. The period between the starting timing of VSE decrease and the timing VSE terminal crossing down to 0.3V is error time (ΔT). Therefore error occurs in output current control.
Iout = 1 / 2 * Np / Ns * Ipk1* (Tres + ΔT) / Tc (10)

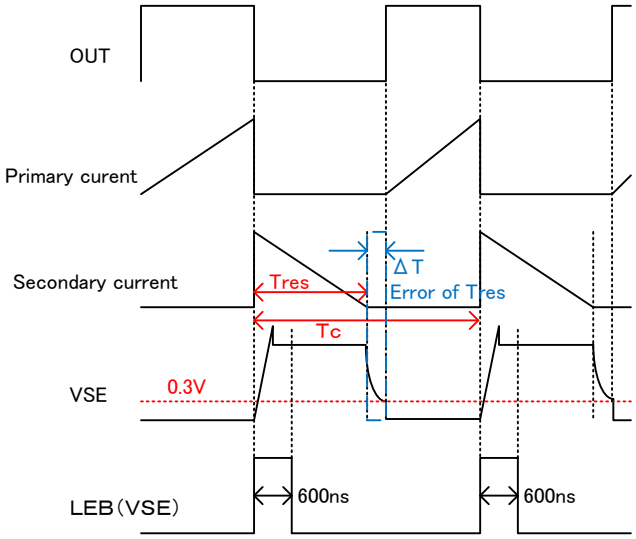


Fig.10 VSE waveform

When FET turns ON, voltage arise in secondary and auxiliary winding in accordance with primary winding voltage and winding turns ratio. Negative voltage of - VIN * Ns / Np arise at auxiliary winding.
When there is no prevention, negative voltage of - VIN * Ns / Np * Rovp2 / (Rovp1 + Rovp2) arise at VSE terminal. But there is a function to reduce the negative voltage near GND level by shorting VSE and GND with a switch inside the IC.
At either of the condition shown below, VSE and GND shorting switch turns on.
1. OUT = Hi
2. Leading Edge Blanking (LED) = Lo and VSE < 0.3.
At the condition shown below, VSE and GND shorting switch turns off.
1. OUT = Lo and VSE > 0.3V

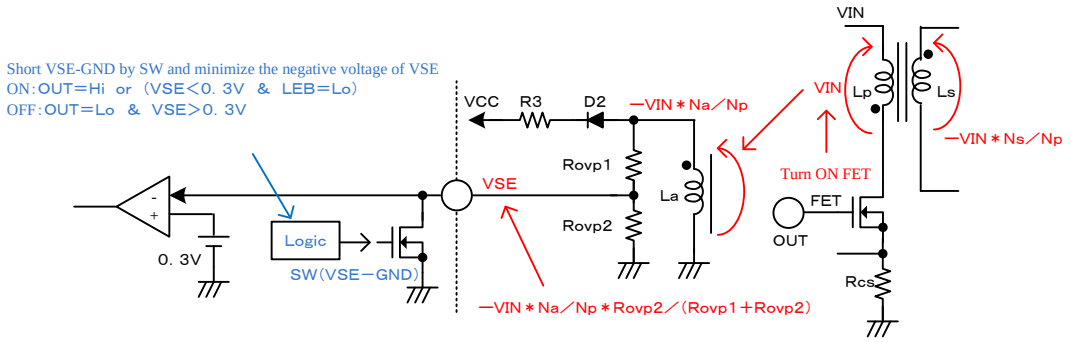


Fig.11 VSE−GND short SW

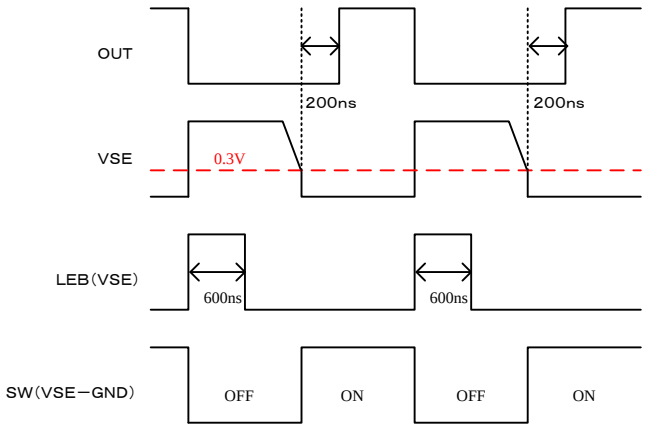


Fig.12 Waveform of VSE − GND short SW

7.4 Peak current detecting circuit (ISE)

ISE terminal is made to detect peak current of primary winding current when FET is ON.
ISE terminal is connected to the source of FET, and current detecting resistor Rcs is connected between the source of FET and GND. The period ISE terminal detects the peak current starts from the timing 200ns before OUT turns off, and end at the timing OUT turns off. It holds the peak amount during the period FET is OFF.

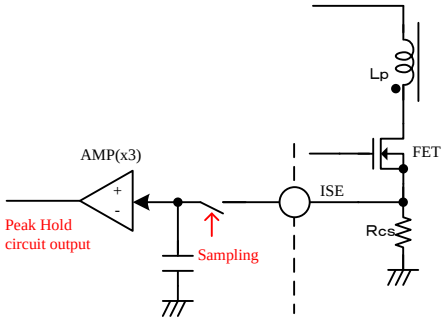


Fig.13 Peak detecting circuit of primary current

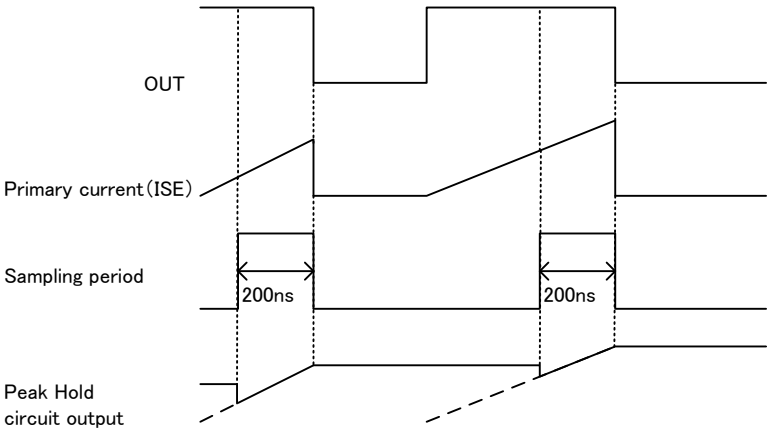


Fig.14 Peak detecting waveform of primary current

7.5 Multiplier (FL1)

FL1 is an output of a Multiplier and is also input of Error Amplifier (EAMP).
The peak hold circuit output VHOLD = Ipk1 * Rcs is divided to Tres / Tc at multiplier.
VFL1 = Ipk1 * Rcs * Tres / Tc (11)
When VFL1 < Vref, EAMP increase the output, and then FET ON period increase, Ipk1 increase, and VFL1 get close to Vref.
When VFL1 > Vref, EAMP decrease the output, and then FET ON period decrease, Ipk1 decrease, and VFL1 get close to Vref.
Therefore error amplifier (EAMP) controls VFL1 to get close to Vref.
VFL1 = Vref = Ipk1 * Rcs * Tres / Tc
Iout = 1 / 2 * Np / Ns * Ipk1 * Tres / Tc
= 1 / 2 * Np / Ns * Vref / Rcs (12)
The equation above means that the three constant (Np, Ns, Rcs) set the output current (Iout).

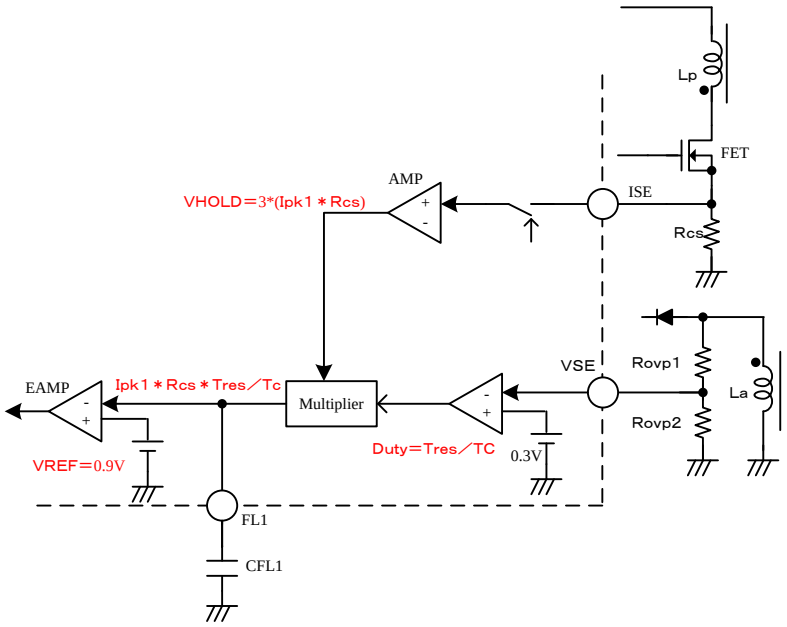


Fig.15 Multiplier (FL1)

When it is non-insulated step up circuit, the equation will be as shown below, since Np=Ns=1.
Iout = 1 / 2 * Vref / Rcs (13)

If CFL1 is a rather large value, the stable control is obtained.
But if CFL1 is too large, the overshoot of FL2 at start up will be large, and overshoot of output current will be large.

Recommended value : 0.1uF≦CFL1≦0.47uF, CFL1≦CFL2

7.6 Error amplifier circuit (FL2)

FL2 is an output of error amplifier (EAMP).
The voltage of FL2 terminal sets FET ON period. As shown in Fig. 18, ON period is as shown below.
ON period = 2.66pF * VFL2 / ibias (14)
Variation range of VFL2 is 0.5V to 4.5V, and on period is 0.66us to 6.00us at Ibias=2uA.

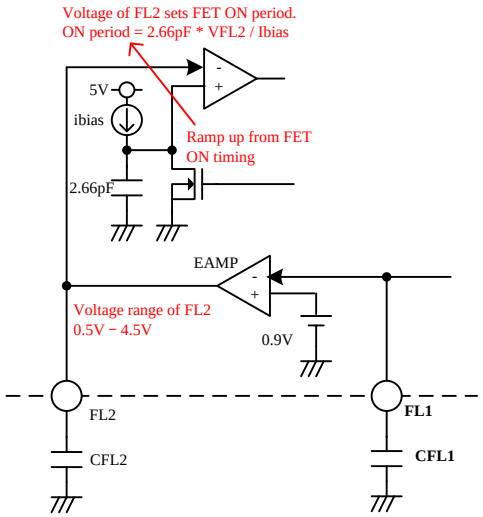


Fig.16 FET ON period control by error amplifier

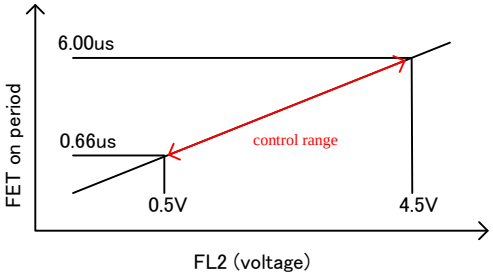


Fig.17 Relation between FL2 voltage and FET on period

As FL2 output is clamped on the maximum voltage 4.5V, on period increases no more. This limits input AC currents when power supply voltage falls rapidly, which is brownout function.

Please decide CFL2 to make ON period constant relative to AC cycle.
If CFL2 is a rather large value, the stable control is obtained.
If CFL2 is too large, the time until LED current starts to flow will be long, when starting up.

7.7 Mode detection circuit (FUNC)

Operational mode can be detected by FUNC pin.
FUNC pin becomes flyback mode above 3.2V.
Since the pull-up of the FUNC pin by constant current of 10uA, it becomes the flyback mode by making a pin open.
When you use it as step down mode, please connect 200kohm between a pin and GND.
Although the resistance connected permits the accuracy of less than 5% of variation, and less than 100 ppm/°C of temperature characteristics, it recommends the accuracy of less than 1% of variation, and less than 100 ppm/°C of temperature characteristics.
When you use it as stanby mode, please set a terminal as GND.
* Step down operation is unidentified.

FUNC pin	Setting	Operation mode
4.5V＞FUNC＞3.2V 2.85V＞FUNC＞1.45V 0.8V＞FUNC	open 200kΩ GND	Flyback Stepdown stanby

(※) It is necessary to input the voltage beyond 1.3V into the return from standby mode at FUNC terminal.

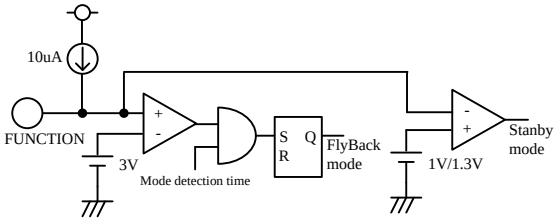


Fig.18 Mode detection by FUNCTION pin

8. Setting operation mode

It is possible to set various operation mode by setting terminals as below table.
Either insulated or non-insulated circuit is capable.
Insulated circuit uses flyback converter method. Non-insulated circuit uses step up or step down converter method with transformer, Furthermore it can realize non-insulated choke coil method, and is able to make thin power supply module without transformer, which is suitable for tube type LED lighting.

insulated / non-insulated	Mode	Terminal setting		
		FL1 pin	FL2 pin	FUNC pin
insulated	Flyback	0.1 ~ 1uF	0.2 ~ 2uF	OPEN
non-insulated	Stepup	0.1 ~ 1uF	0.2 ~ 2uF	OPEN
non-insulated	Stepdown	0.1 ~ 1uF	0.2 ~ 2uF	200kΩ
insulated / non-insulated	stanby	—	—	0V

※A step-up system is unidentified.

8.1 Flyback mode

Fig. 19 shows circuit diagram of insulated flyback mode.

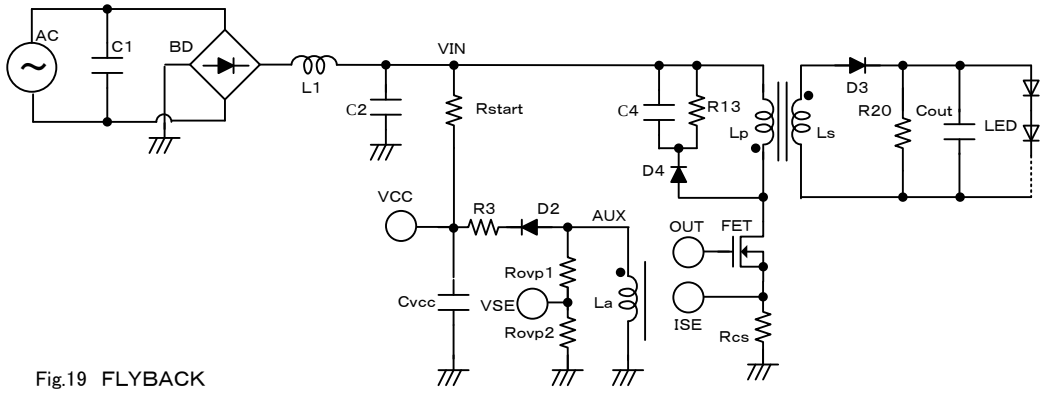


Fig.19 FLYBACK

8.2 Non-insulated mode (transformer : step up)

Fig. 20 shows circuit diagram of non-insulated step up mode with transformer. Snubber circuit is not necessary and there is no loss of Lp leakage inductance in this mode compared to in flyback method.
※A step-up system is unidentified.

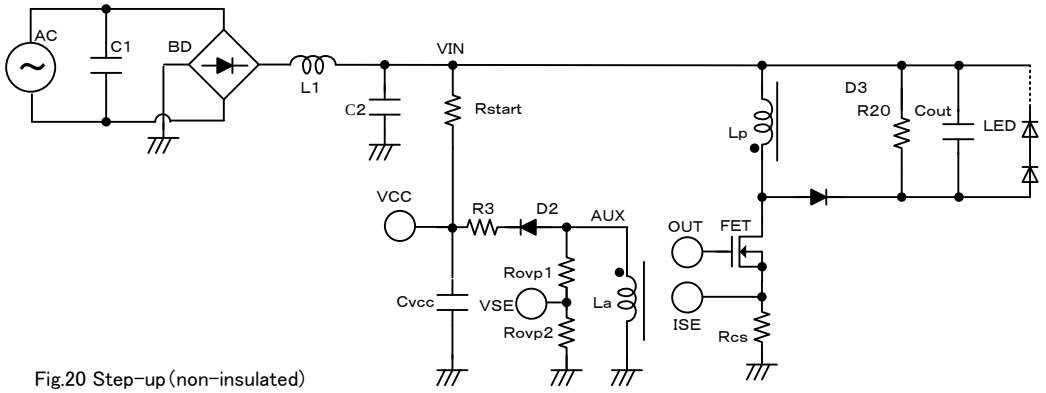


Fig.20 Step-up(non-insulated)

8.3 Non-insulated mode (transformer : step down)

Fig. 21 shows circuit diagram of non-insulated step-down mode with transformer. Peak current of LED can be reduced in this mode compared to in step up mode.

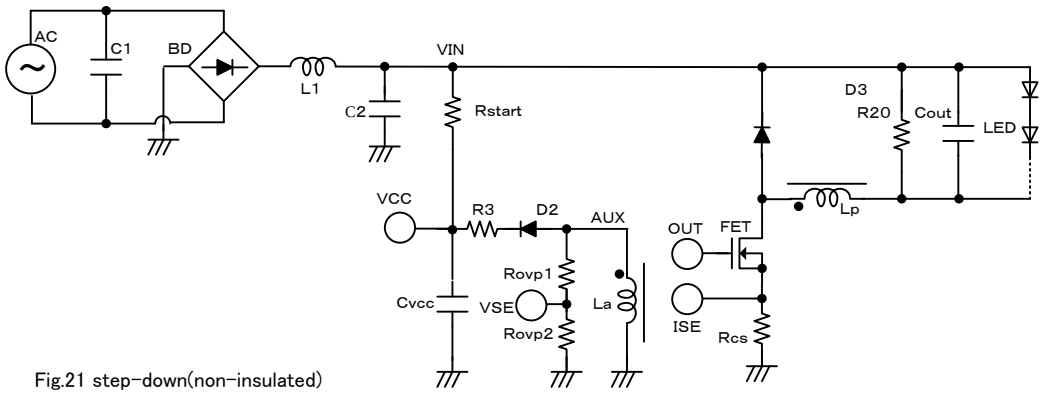


Fig.21 step-down(non-insulated)

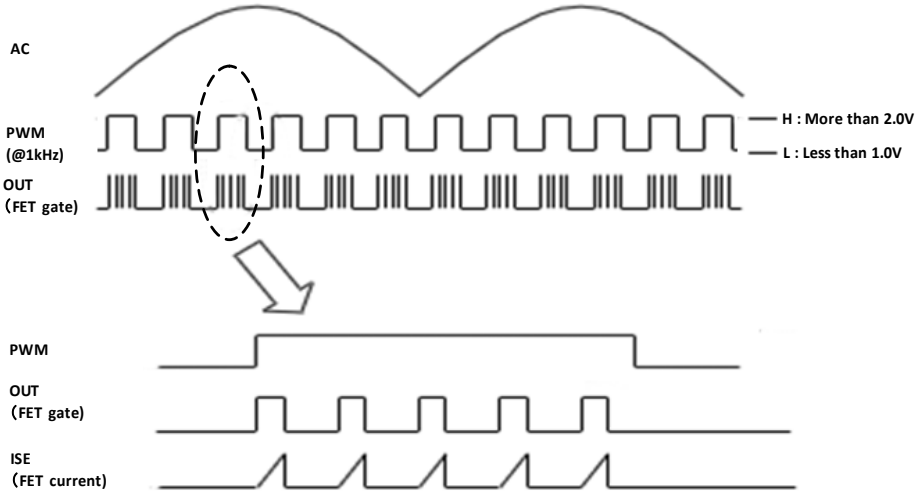
8.4 PWM Dimmer function

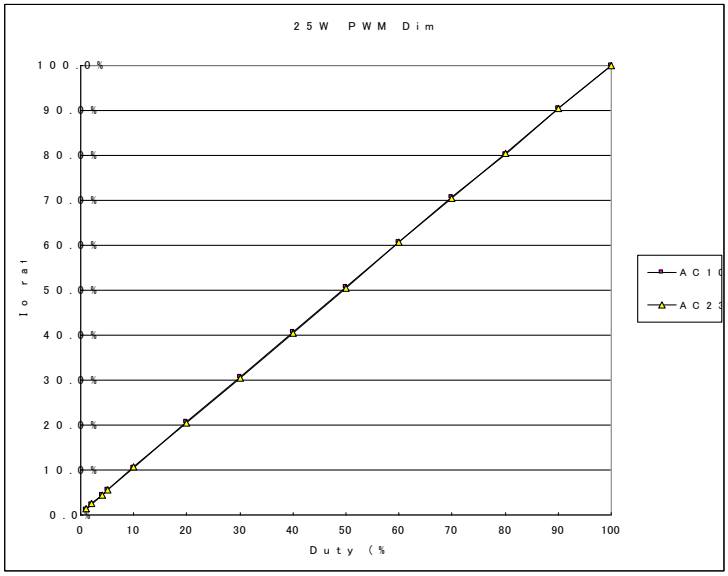
LED current can be adjusted according to Duty of PWM pulse input to FUNC pin.
Please input a PWM signal after the mode judging of the 7.7th clause of operation.
In example fly back operation, High of a PWM signal is inputted after a judgment of operation by 3.2 V < FUNC < 4.5V.
Normal operation is carried out when a PWM pulse is in a high state (1.45V to 4.5V).
Switching operation is stopped when a PWM pulse is in a low state (under 0.8V).

FUNC pin setting (@1kHz)	Dimming result
4.5V ＞ FUNC ＞ 1.45V	Out pin : switching
0.8V ＞ FUNC	Out pin : OFF (※2)

(※2) In FUNC < 0.8V, the value of FL1 and FL2 is kept and the switching-on pulse is kept constant.

When a PWM function is used, please use it after are satisfactory or checking enough with the system, since sound may occur with a transformer, a coil, etc.





9. Protection Function

9.1 Soft start function

At start up, switching operation is performed in soft start sequence. On time and off time shown at below table are repeated in turns until condition of StartupOK.
On timing : ISE=0.6V or Ton(Max.)=6us
Off period : Critical Current Mode operation, Toff (Min.)=12 us or more
Condition of Startup OK : VSE > 0.8V.

At stepdown mode soft start condition is as below.
On timing : ISE=0.3V or Ton(Max.)=6us
Off period : Critical Current Mode operation, Toff (Min.)=12 us or more
Condition of Startup OK : VSE > 0.8V

Mode	Soft start	Startup OK judge
Flyback	ON : ISE = 0.6V, Ton(max) = 6us OFF : Critical Current Mode operation, Toff(min) = 12us	VSE = 0.8V
Stepdown	ON : ISE = 0.3V, Ton(max) = 6us OFF : Critical Current Mode operation, Toff(min) = 12us	VSE = 0.8V

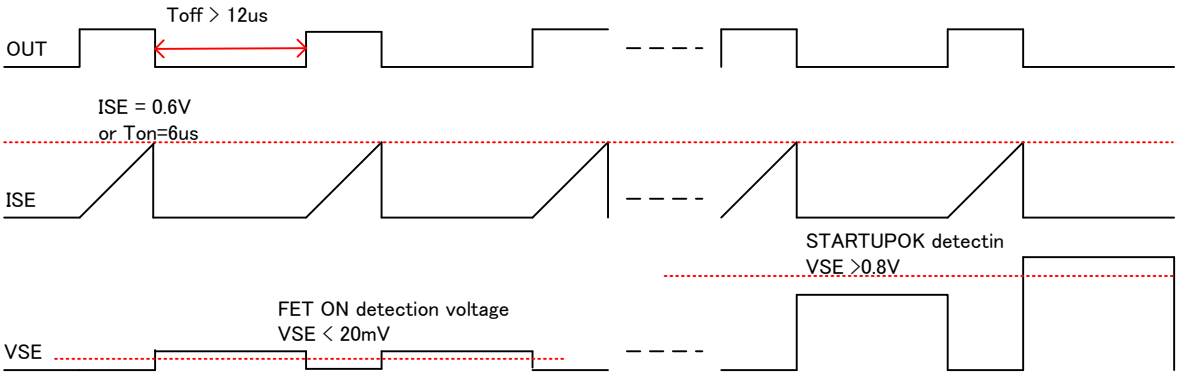


Fig.22 Softstart

9.2 Over temperature protection

When junction temperature of this IC exceeds 150°C, over temperature protection (OHP) starts to operate and following operation is performed.

・ IC shut down (OUT is Lo, shut down 3V regulator inside the IC).

・ Discharge capacitor connected to FL2 (CFL2).

・ Discharge capacitor connected to VCC (Cvcc).

・ When VCC goes down to UVLO (Typ.6V) or less, discharge of Cvcc stops.

Fig.23 shows the fail safe circuit .

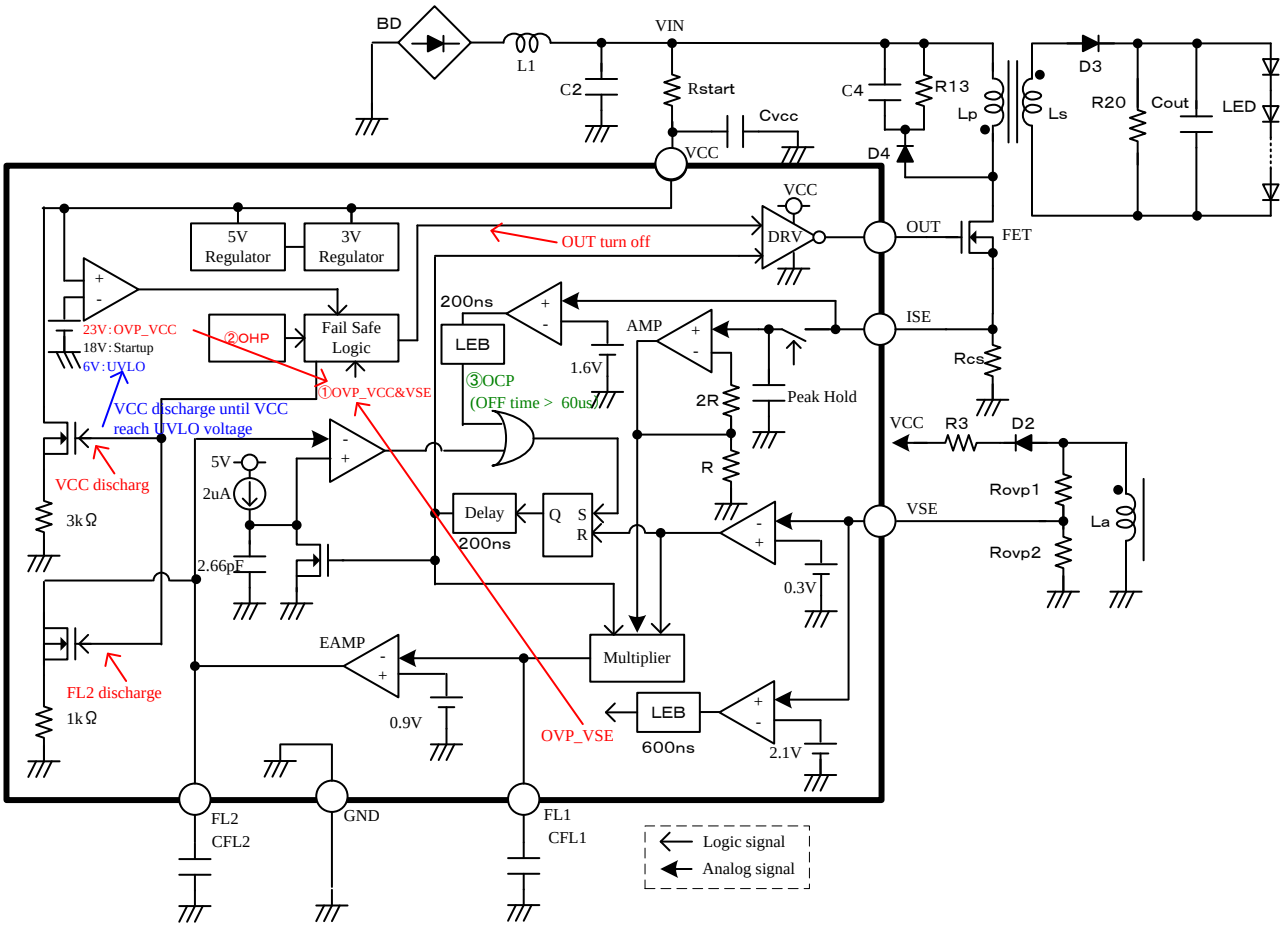


Fig.23 FailSafe

9.3 VCC under voltage lock-out

IC operation stops when VCC voltage goes down to Typ.6V or less, caused by VCC voltage lowering or short between VCC and GND.
IC operation restarts when VCC voltage goes up to Typ.18V or more (start up voltage).

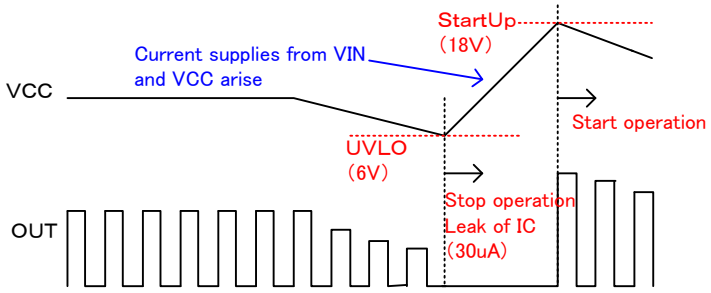


Fig.24 UVLO detection sequence

9.4 Output over voltage lock-out

When over voltage error is detected, following operation is performed.

・ IC shut down (OUT is Lo, shut down 3V regulator inside the IC).

・ Discharge capacitor connected to FL2 (CFL2).

・ Discharge capacitor connected to VCC (Cvcc).

・ When VCC goes down to UVLO (Typ.6V) or less, discharge of Cvcc stops.

The fail safe circuit is as shown in Fig. 23.
Over voltage protection is masked at Leading edge blanking (LEB) period, that is 600ns (Typ.) from the timing OUT becomes Lo (Fig. 25).
Over voltage protection is detected by V_{OVP_VSE} ≧ 2.1V (Typ.) (15), and V_{OVP_VCC} ≧ 22.7 (Typ.) (16).

$$V_{OVP\_VSE} = Ns / Na * (Rovp1 + Rovp2) / Rovp2 * V_{OVP\_VSE} \quad (15)$$

$$V_{OVP\_VCC} = Ns / Na * V_{OVP\_VCC} \quad (16)$$

※Vovp_vse is over voltage threshold voltage for VSE. Vovp_VCC is over voltage threshold voltage for VCC.

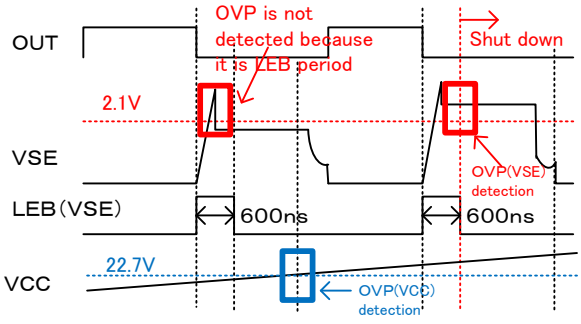


Fig.25 OVP detection

9.5 FET over current protection

The IC observe FET ON current, and when ISE goes up to over current threshold voltage (Vocp) or more, over current error is detected and following operation is performed.

- OUT turns Lo and stops switching.
- IC do not shut down.
- OFF period will be more than 67us (Typ.).

The voltage of ISE terminal at over-current detection is as follows.

Mode	over-current detection volgate
Flyback	ISE ≦1.6V(Typ.)
Step-down	ISE ≦0.8V(Typ.)

Over current protection is masked at leading edge blanking (LEB) period, that is 200ns (Typ.) from the timing OUT becomes Hi (Fig. 26).
When OCP is detected, OFF period is set to be 67us (Typ.).

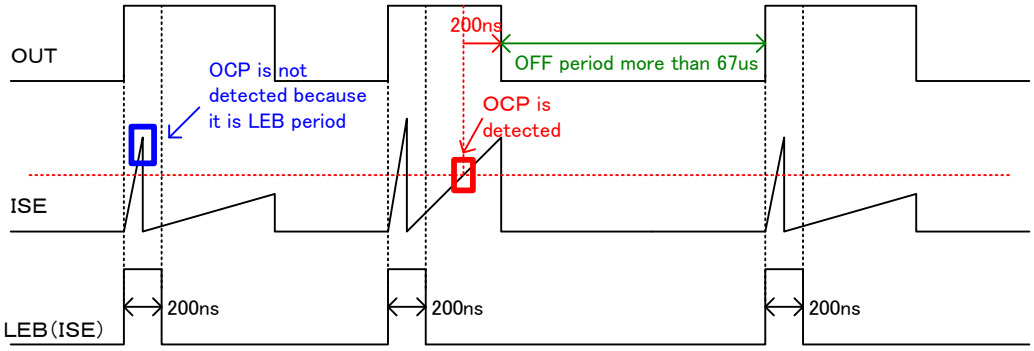


Fig.26 OCP detection

10. External circuit example

10.1 Transformer

First you must fix the input condition of AC power source
VAC : 85V (Min.) ~ 265V (Max.)
Fix inductance of primary winding of transformer (Lp) to make ON period 6 us at the condition VAC (Min.).
Lp = VAC (Min.) * Ton / Ip (17)
When duty is 50%, since AC input current is IAC = Ip / 4, Ip can be expressed as below
Ip = 4 * Pin / VAC (Min.) (18)
IAC = Ip / 4 (19)

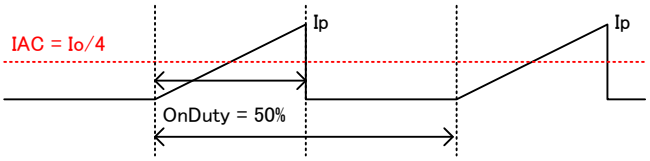


Fig.27

Pin and Pout can be expressed as below, using conversion efficiency η
Pin = Pout / η (20)

When VAC (Min.) = 85V, Ton = 6us, Pout = 6.4W, and efficiency η = 85%
Pin = 6.4W / 85% = 7.43W
Ip = 4 * 7.43W / 85V = 0.35A
Lp = 85V * 6us / 0.35A = 1.37m^{2}H

・ Primary widing
Np = VAC (Min.) * Ton (Max.) / (Ae * BT) (21)
Use the larger amount between
Vin (Min.) * Ton (Max.) or Vin (Max.) * Ton (Min.)
Ae is the effective area of the core in transformer.
BT is saturation flux density.
Use EE15 core (Ae = 15mm^2), calculate using saturation flux density BT = 320mT
Np = 85V * √2 * 6us / (15mm^2 * 320mT)
= 150.3
Set Np more than the value above.

・ Ns (Secondary winding turns)
Ns = Np * Vout / VAC (Min.) (22)
When Np = 150, Vout = 35.5V, VAC (Min.) = 85V
Ns = 150 * 35.5V / 85V = 62.6
Therefore Ns = 63

・ Na (Auxiliary widing turns)
Make VCC voltage more than 16V.
Na = Ns * VCC / Vout (23)
=63 * 16V / 35.5V = 28.4
Therefore Na = 28

・ Winding form

Voltage change of primary winding make an effect on auxiliary winding, in accordance with magnetic coupling strength of primary winding and auxiliary winding.
It is able to weaken magnetic coupling by changing winding form, and weaken the effect on auxiliary winding.

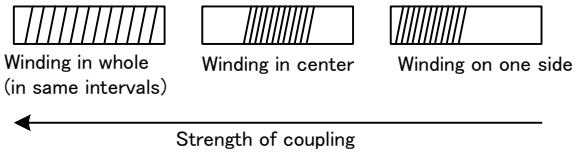


Fig.27 Strengh of coupling between primary winding and auxiliary winding for each winding form of auxiliary winding.

10.2 FET

Please use FET with a sufficient margin against primary winding peak current, and drain voltage rising at FET OFF.
When the gate of FET change from Hi to Lo, negative surge is applied to the source of FET.
Because there is parasitic capacitance between the gate and the source of FET.

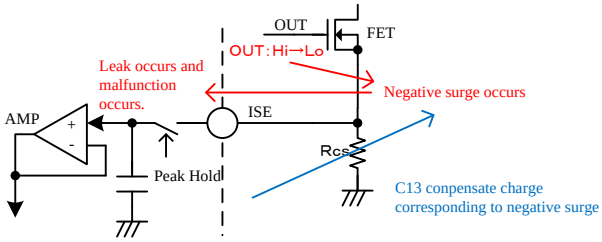


Fig.28 Counter measure against negative surge

10.3 Snubber circuit

When using insulated flyback circuit, you must consume the energy of leakage inductance caused by imperfect magnetic coupling of transformer at the primary winding.

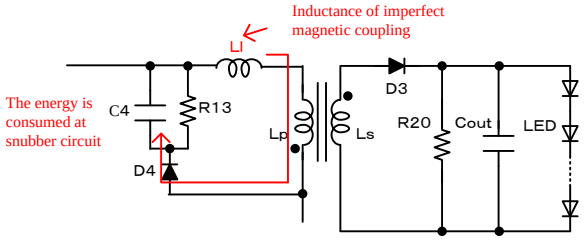


Fig.29 Snubber circuit

Appropriate value of C4 and R13 is set to keep voltage jumping of the drain at low level.

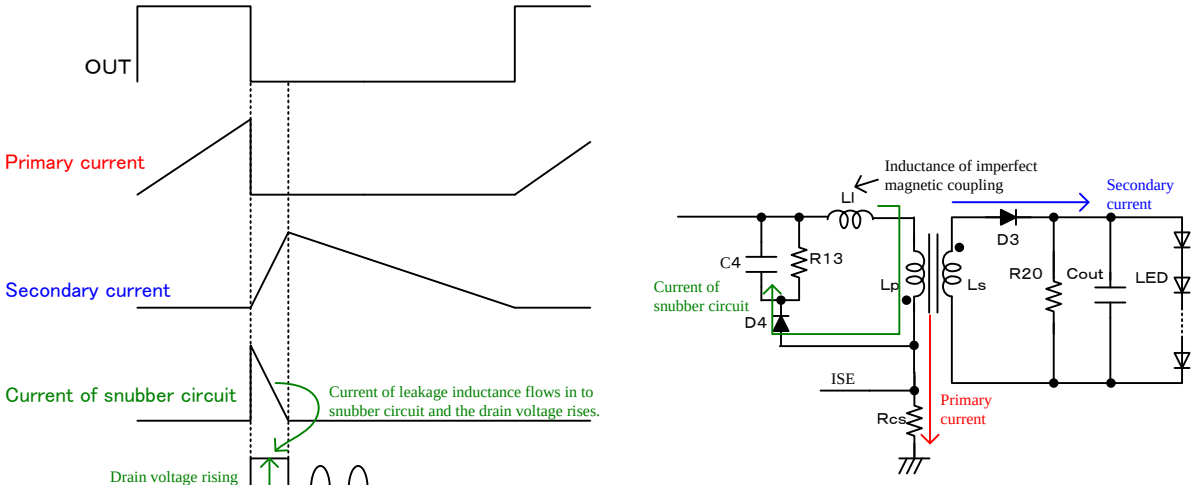


Fig.30 Drain voltage rising caused by leakage inductance

10.4 Filter circuit

The value of L1 and C2 is set by EMI observation. The cut off frequency of low pass filter made by L1 and C1 is as shown below.
fc = 1 / (2π √(L1 * C2)) (24)

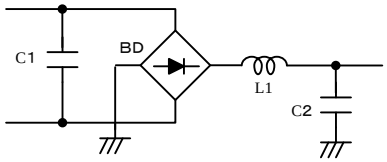
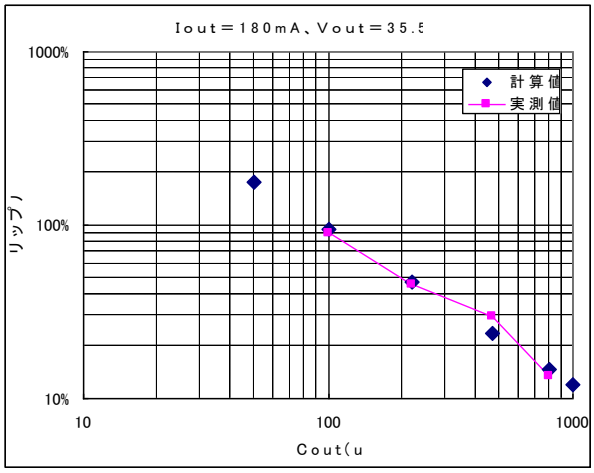
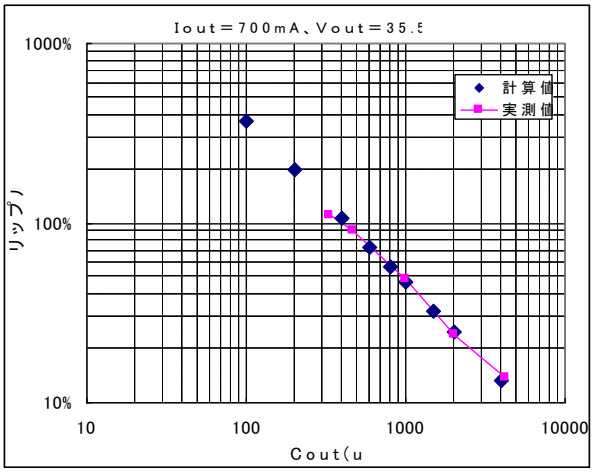


Fig.31 LC filter

10.5 Output capacitor

A large value of output capacitor (Cout) is needed to keep output current ripple at low level.
At the condition of power factor more than 0.9, the output ripple is approximately as shown below.
Output ripple rate = Iout / 3 * Cout ^ - 0.9 (25)
Where Iout is output current





11 Notes on Contents

1) Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2) Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3) Timing Charts
Timing charts may be simplified for explanatory purposes.

4) Application Circuits
The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
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